Nuvoton 1T 8051-based Microcontroller

N76E003

Datasheet

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1. GENERAL DESCRIPTION

The N76E003 is an embedded flash type, 8-bit high performance 1T 8051-based microcontroller. The instruction set is fully compatible with the standard 80C51 and performance enhanced.

The N76E003 contains a up to 18K Bytes of main Flash called APROM, in which the contents of User Code resides. The N76E003 Flash supports In-Application-Programming (IAP) function, which enables on-chip firmware updates. IAP also makes it possible to configure any block of User Code array to be used as non-volatile data storage, which is written by IAP and read by IAP or MOVC instruction. There is an additional Flash called LDROM, in which the Boot Code normally resides for carrying out In-System-Programming (ISP). The LDROM size is configurable with a maximum of 4K Bytes. To facilitate programming and verification, the Flash allows to be programmed and read electronically by parallel Writer or In-Circuit-Programming (ICP). Once the code is confirmed, user can lock the code for security.

The N76E003 provides rich peripherals including 256 Bytes of SRAM, 768 Bytes of auxiliary RAM (XRAM), Up to 18 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, one SPI, one I^2C, five enhanced PWM output channels, eight-channel shared pin interrupt for all I/O, and one 12-bit ADC. The peripherals are equipped with 18 sources with 4-level-priority interrupts capability.

The N76E003 is equipped with three clock sources and supports switching on-the-fly via software. The three clock sources include external clock input, 10 kHz internal oscillator, and one 16 MHz internal precise oscillator that is factory trimmed to ±1% at room temperature. The N76E003 provides additional power monitoring detection such as power-on reset and 4-level brown-out detection, which stabilizes the power-on/off sequence for a high reliability system design.

The N76E003 microcontroller operation consumes a very low power with two economic power modes to reduce power consumption — Idle and Power-down mode, which are software selectable. Idle mode turns off the CPU clock but allows continuing peripheral operation. Power-down mode stops the whole system clock for minimum power consumption. The system clock of the N76E003 can also be slowed down by software clock divider, which allows for a flexibility between execution performance and power consumption.

With high performance CPU core and rich well-designed peripherals, the N76E003 benefits to meet a general purpose, home appliances, or motor control system accomplishment.

2. FEATURES

- CPU:
  - Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller.
  - Instruction set fully compatible with MCS-51.
  - 4-priority-level interrupts capability.
  - Dual Data Pointers (DPTRs).
- Operating:
  - Wide supply voltage from 2.4V to 5.5V.
  - Wide operating frequency up to 16 MHz.
  - Industrial temperature grade: -40℃ to +105℃.
- Memory:
  - Up to 18K Bytes of APROM for User Code.
  - Configurable 4K/3K/2K/1K/0K Bytes of LDROM, which provides flexibility to user developed Boot Code.
  - Flash Memory accumulated with pages of 128 Bytes each.
  - Built-in In-Application-Programmable (IAP).
  - Code lock for security.
  - 256 Bytes on-chip RAM.
  - Additional 768 Bytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
- Clock sources:
  - 16 MHz high-speed internal oscillator trimmed to ±1% when V_{DD} 5.0V, ±2% in all conditions.
  - 10 kHz low-speed internal oscillator.
  - External clock input.
  - On-the-fly clock source switch via software.
  - Programmable system clock divider up to 1/512.
- Peripherals:
  - Up to 17 general purpose I/O pins and one input-only pin. All output pins have individual 2-level slew rate control.
  - Standard interrupt pins $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$.
  - Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051.

  - One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected.
  - One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.
  - One 16-bit PWM counter interrupt for timer.
  - One programmable Watchdog Timer (WDT) clocked by dedicated 10 kHz internal source.
  - One dedicated Self Wake-up Timer (WKT) for self-timed wake-up for power reduced modes.
  - Two full-duplex UART ports with frame error detection and automatic address recognition. TXD and RXD pins of UART0 exchangeable via software.
  - One SPI port with master and slave modes, up to 8 Mbps when system clock is 16 MHz.
  - One I^2C bus with master and slave modes, up to 400 kbps data rate.
  - Three pairs, six channels of pulse width modulator (PWM) output, 10 output pins can be selected., up to 16-bit resolution, with different modes and Fault Brake function for motor control.
  - Eight channels of pin interrupt, shared for all I/O ports, with variable configuration of edge/level detection.
  - One 12-bit ADC, up to 500 ksps converting rate, hardware triggered and conversion result compare facilitating motor control.
- Power management:
  - Two power reduced modes: Idle and Power-down mode.
- Power monitor:
  - Brown-out detection (BOD) with low power mode available, 4-level selection, interrupt or reset options.
  - Power-on reset (POR).
- Strong ESD and EFT immunity.
- Development Tools:
  - Nuvoton On-Chip-Debugger (OCD) with KEIL™ development environment.
  - Nuvoton In-Circuit-Programmer (ICP).
  - Nuvoton In-System-Programming (ISP) via UART.

- Part numbers and packages:

Part Number	APROM	LDROM	Package
N76E003AT20	18K Bytes shared with LDROM	Up to 4K Bytes	TSSOP 20
N76E003AQ20	18K Bytes shared with LDROM	Up to 4K Bytes	QFN 20

3. BLOCK DIAGRAM

Figure 3-1 shows the N76E003 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

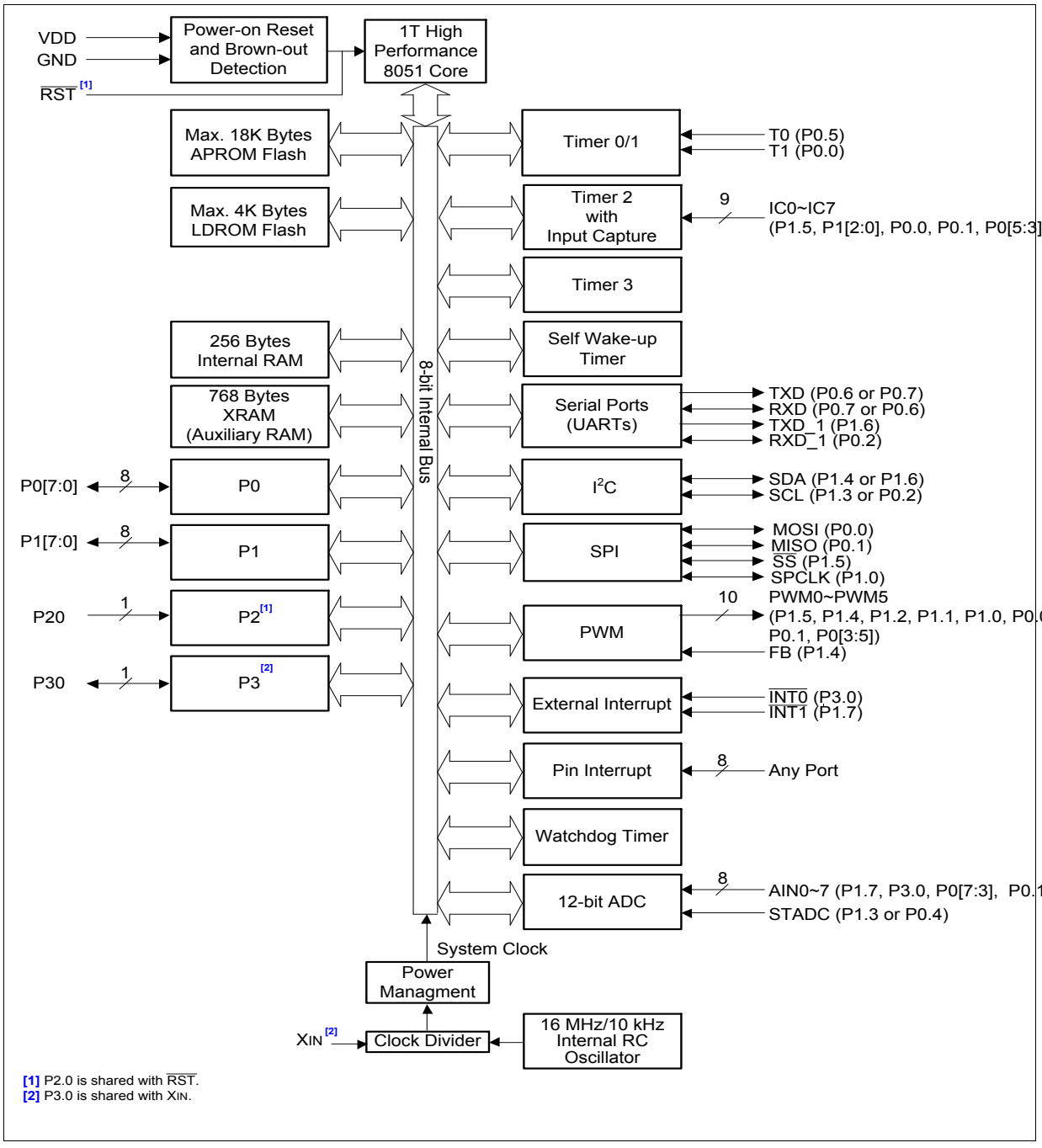
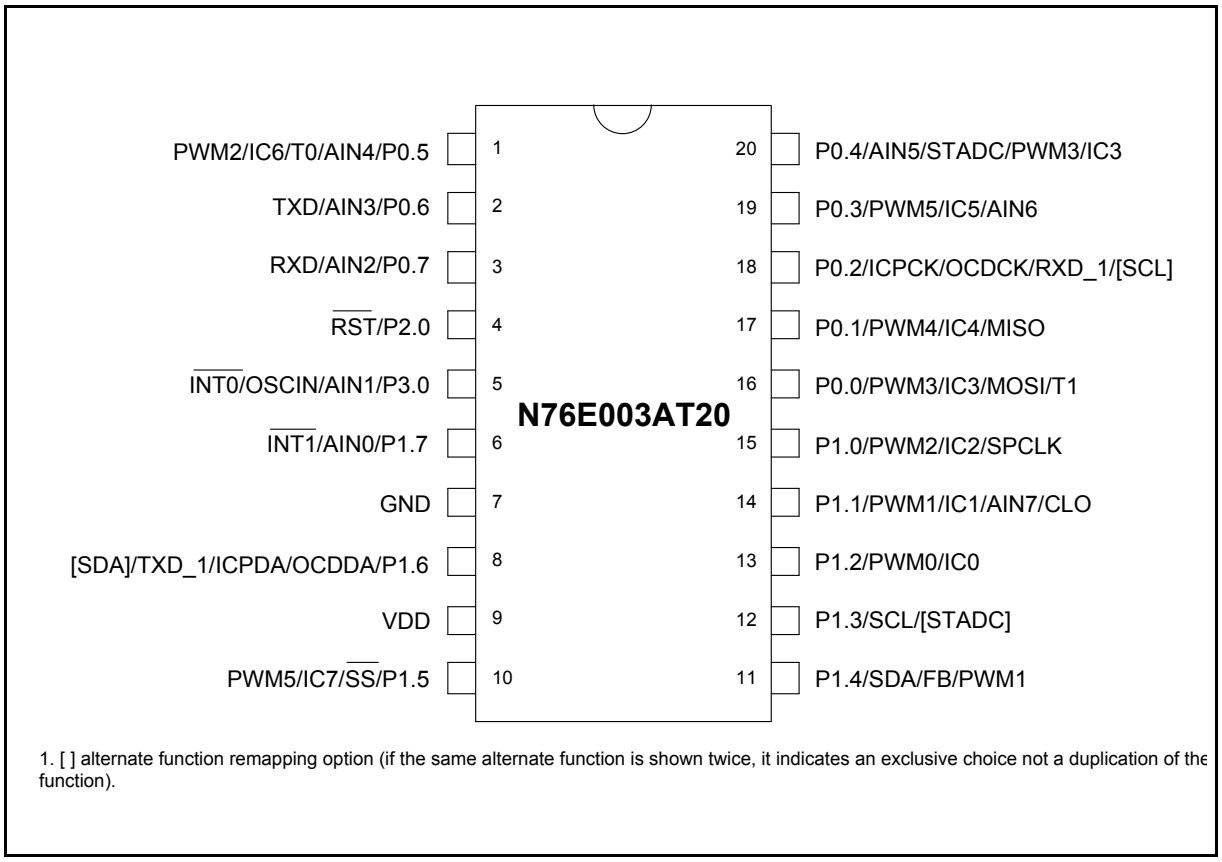


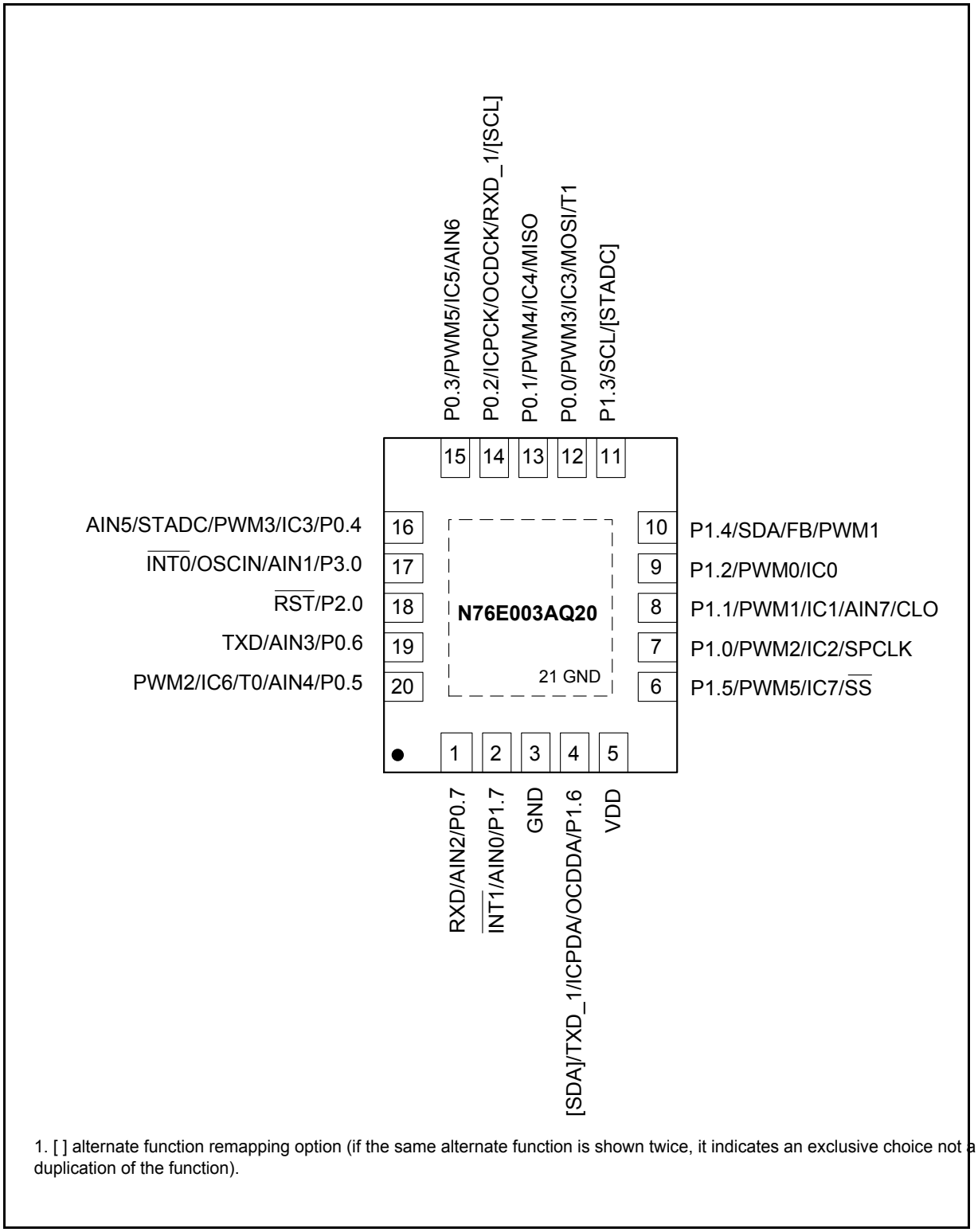
Figure 3-1. Functional Block Diagram

4. PIN CONFIGURATION



1. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4-1. Pin Assignment of TSSOP-20 Package



1. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4-2. Pin Assignment of QFN-20 Package

Pin Number		Symbol	Multi-Function Description[1]
TSSOP20	QFN20		
9	5	VDD	**POWER SUPPLY:** Supply voltage V_{DD} for operation.
7	3	GND	**GROUND:** Ground potential.
16	12	P0.0/PWM3/IC3/MOSI/T1	**P0.0:** Port 0 bit 0.
			PWM3: PWM output channel 3.
			MOSI: SPI master output/slave input.
			IC3: Input capture channel 3.
			T1: External count input to Timer/Counter 1 or its toggle output.
17	13	P0.1/PWM4/IC4/MISO	**P0.1:** Port 0 bit 1.
			PWM4: PWM output channel 4.
			IC4: Input capture channel 4.
			MISO: SPI master input/slave output.
18	14	P0.2/ICPCK/OCDCK/RXD_1 /[SCL]	**P0.2:** Port 0 bit 2.
			ICPCK: ICP clock input.
			OCDCK: OCD clock input.
			RXD_1: Serial port 1 receive input.
			[SCL][3]**:** I^2C clock.
19	15	P0.3/PWM5/IC5/AIN6	**P0.3:** Port 0 bit 3.
			PWM5: PWM output channel
			IC5: Input capture channel 5.
			AIN6: ADC input channel 6.
20	16	P0.4/AIN5/STADC/PWM3/ IC3	**P0.4:** Port 0 bit 4.
			AIN5: ADC input channel 5.
			STADC: External start ADC trigger
			PWM3: PWM output channel 3.
			IC3: Input capture channel 3.
1	20	P0.5/PWM2/IC6/T0/AIN4	**P0.5:** Port 0 bit 5.
			PWM2: PWM output channel 2.
			IC6: Input capture channel 6.
			T0: External count input to Timer/Counter 0 or its toggle output.
2	19	P0.6/TXD/AIN3	**P0.6:** Port 0 bit 6.
			TXD[2]**:** Serial port 0 transmit data output.
			AIN3: ADC input channel 3.
3	1	P0.7/RXD/AIN2	**P0.7:** Port 0 bit 7.
			RXD: Serial port 0 receive input.
			AIN2: ADC input channel 2.
15	7	P1.0/PWM2/IC2/SPCLK	**P1.0:** Port 1 bit 0.
			PWM2: PWM output channel 2.
			IC2: Input capture channel 2.
			SPCLK: SPI clock.
14	8	P1.1/PWM1/IC1/AIN7/CL O	**P1.1:** Port 1 bit 1
			PWM1: PWM output channel 1.
			IC1: Input capture channel 1.
			AIN7: ADC input channel 7.
			CLO: System clock output.
13	9	P1.2/PWM0/IC0	**P1.2:** Port 1 bit 2.
			PWM0: PWM output channel 0.
			IC0: Input capture channel 0.
12	11	P1.3/SCL/[STADC]	**P1.3:** Port 1 bit 3.
			SCL: I^2C clock.

Pin Number		Symbol	Multi-Function Description[1]
TSSOP20	QFN20		
			[STADC][4]**:** External start ADC trigger
11	10	P1.4/SDA/FB/PWM1	**P1.4:** Port 1 bit 4.
			SDA: I2C data.
			FB: Fault Brake input.
			PWM1: PWM output channel 1.
10	6	P1.5/PWM5/IC7/SS	**P1.5:** Port 1 bit 5.
			PWM5: PWM output channel 5.
			IC7: Input capture channel 7.
			SS: SPI slave select input.
8	4	P1.6/ICPDA/OCDDA/TXD_1 /[SDA]	**P1.6:** Port 1 bit 6.
			ICPDA: ICP data input or output.
			OCDAT: OCD data input or output.
			TXD_1: Serial port 1 transmit data output.
			[SDA][3]**:** I2C data.
6	2	P1.7/INT1/AIN0	**P1.7:** Port 1 bit 7.
			INT1: External interrupt 1 input.
			AIN0: ADC input channel 0.
4	18	P2.0/RST	**P2.0:** Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
			RST: RST pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
5	17	P3.0/INT0/OSCIN/AIN1	**P1.0:** Port 3 bit 0 available when the internal oscillator is used as the system clock.
			INT0: External interrupt 0 input.
			XIN: If the ECLK mode is enabled, XIN is the external clock input pin.
			AIN1: ADC input channel 1.

[1] All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description. See Section 16. "Pin Interrupt".
[2] TXD and RXD pins of UART0 are software exchangeable by UART0PX (AUXR1.2).
[3] [I2C] alternate function remapping option. I2C pins is software switched by I2CPX (I2CON.0).
[4] [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).
[5] PIOx register decides which pins are PWM or GPIO.

5. MEMORY ORGANIZATION

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In N76E003, there are 256 Bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the N76E003 provides another on-chip 768 Bytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded flash, functioning as Program Memory, is divided into three blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code, and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 Bytes. The flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes.

5.1 Program Memory

The Program Memory stores the program codes to execute as shown in Figure 5-1. After any reset, the CPU begins execution from location 0000H.

To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the Program Memory. Each interrupt is assigned with a fixed location in the Program Memory. The interrupt causes the CPU to jump to that location with where it commences execution of the interrupt service routine (ISR). External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine should begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

The interrupt service locations are spaced at an interval of eight Bytes: 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within the 8-Byte interval. However longer service routines should use a JMP instruction to skip over subsequent interrupt locations if other interrupts are in use.

The N76E003 provides two internal Program Memory blocks APROM and LDROM. Although they both behave the same as the standard 8051 Program Memory, they play different rules according to

their ROM size. The APROM on N76E003 can be up to 18K Bytes. User Code is normally put inside. CPU fetches instructions here for execution. The MOVC instruction can also read this region.

The other individual Program Memory block is called LDROM. The normal function of LDROM is to store the Boot Code for ISP. It can update APROM space and CONFIG bytes. The code in APROM can also re-program LDROM. For ISP details and configuration bit setting related with APROM and LDROM, see Section 21.4 “In-System-Programming (ISP)” on page 220. Note that APROM and LDROM are hardware individual blocks, consequently if CPU re-boots from LDROM, CPU will automatically re-vector Program Counter 0000H to the LDROM start address. Therefore, CPU accounts the LDROM as an independent Program Memory and all interrupt vectors are independent from APROM.

CONFIG1

7	6	5	4	3	2	1	0
-	-	-	-	-	LDSIZE[2:0]		
-	-	-	-	-	R/W		

Factory default value: 1111 1111b

Bit	Name	Description
2:0	LDSIZE[2:0]	**LDROM size select** This field selects the size of LDROM. 111 = No LDROM. APROM is 18K Bytes. 110 = LDROM is 1K Bytes. APROM is 17K Bytes. 101 = LDROM is 2K Bytes. APROM is 16K Bytes. 100 = LDROM is 3K Bytes. APROM is 15K Bytes. 0xx = LDROM is 4K Bytes. APROM is 14K Bytes.

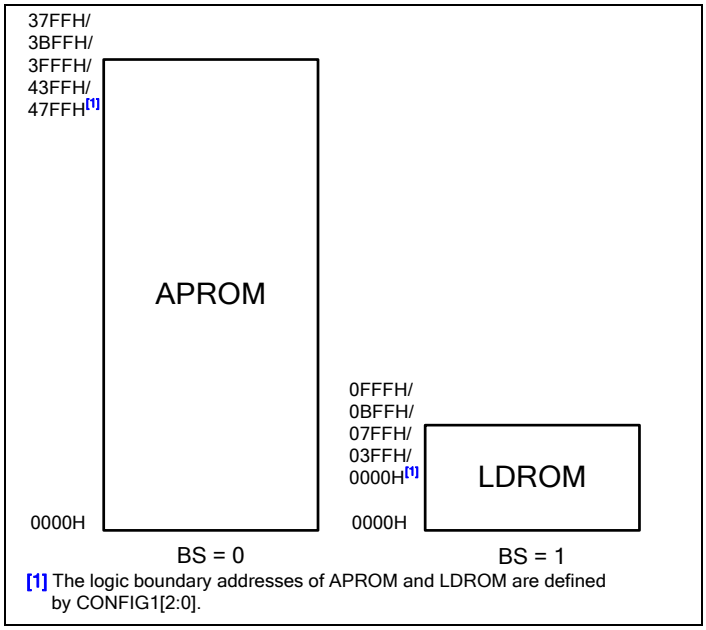


Figure 5-1. N76E003 Program Memory Map

5.2 Data Memory

Figure 5-2 shows the internal Data Memory spaces available on N76E003. Internal Data Memory occupies a separate address space from Program Memory. The internal Data Memory can be divided into three blocks. They are the lower 128 Bytes of RAM, the upper 128 Bytes of RAM, and the 128 Bytes of SFR space. Internal Data Memory addresses are always 8-bit wide, which implies an address space of only 256 Bytes. Direct addressing higher than 7FH will access the special function registers (SFRs) space and indirect addressing higher than 7FH will access the upper 128 Bytes of RAM. Although the SFR space and the upper 128 Bytes of RAM share the same logic address, 80H through FFH, actually they are physically separate entities. Direct addressing to distinguish with the higher 128 Bytes of RAM can only access these SFRs. Sixteen addresses in SFR space are either byte-addressable or bit-addressable. The bit-addressable SFRs are those whose addresses end in 0H or 8H.

The lower 128 Bytes of internal RAM are present in all 80C51 devices. The lowest 32 Bytes as general purpose registers are grouped into 4 banks of 8 registers. Program instructions call these registers as R0 to R7. Two bits RS0 and RS1 in the Program Status Word (PSW[3:4]) select which Register Bank is used. It benefits more efficiency of code space, since register instructions are shorter than instructions that use direct addressing. The next 16 Bytes above the general purpose registers (byte-address 20H through 2FH) form a block of bit-addressable memory space (bit-address 00H through 7FH). The 80C51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Either direct or indirect addressing can access the lower 128 Bytes space. But the upper 128 Bytes can only be accessed by indirect addressing.

Another application implemented with the whole block of internal 256 Bytes RAM is used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a JMP, CALL or interrupt is invoked, the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07H at reset. User can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

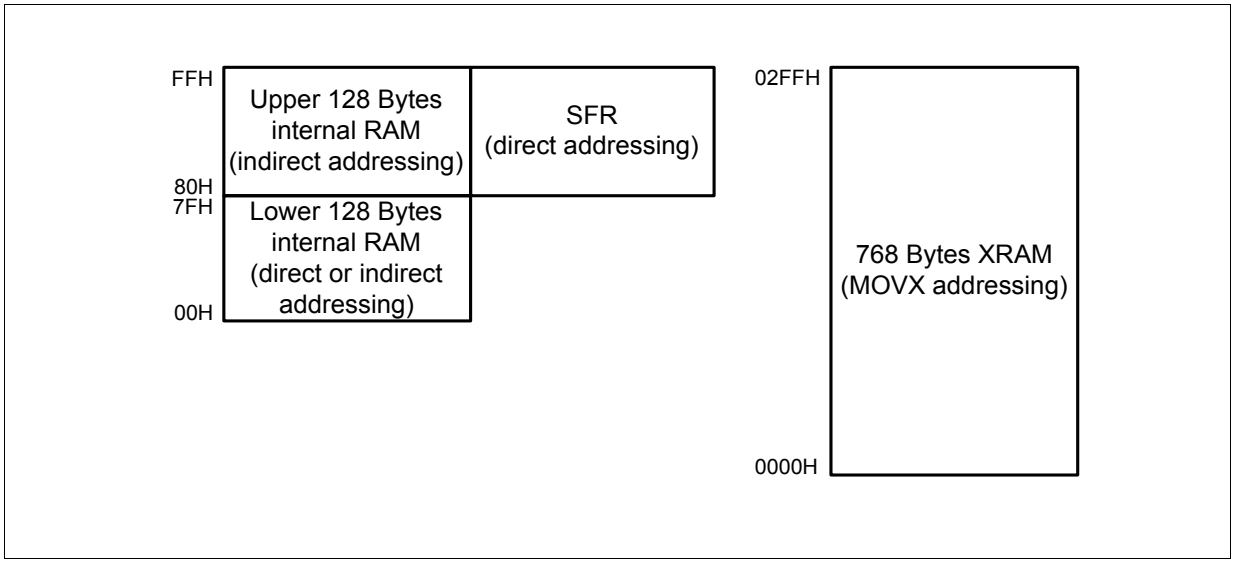


Figure 5-2. Data Memory Map

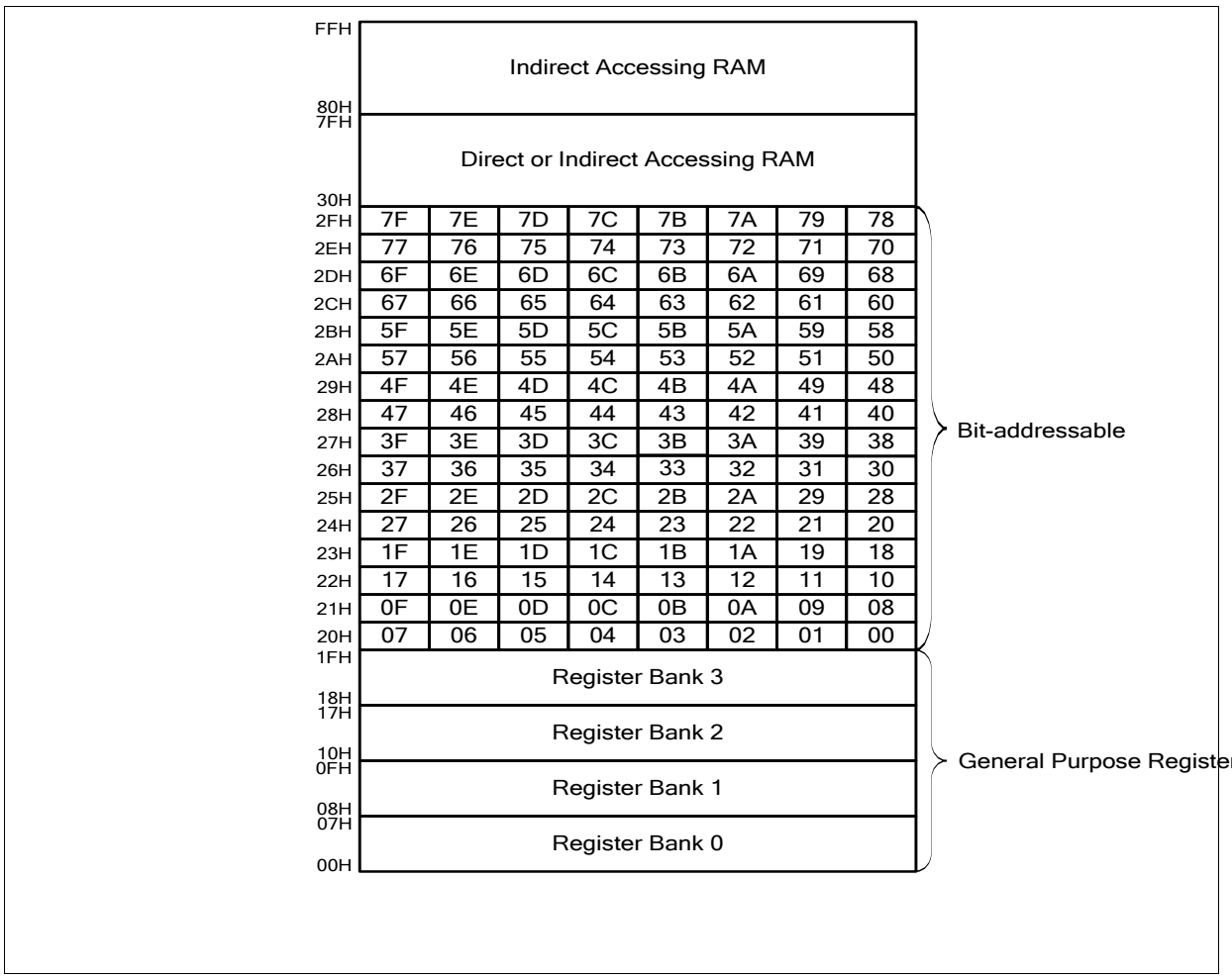


Figure 5-3. Internal 256 Bytes RAM Addressing

5.3 On-Chip XRAM

The N76E003 provides additional on-chip 768 bytes auxiliary RAM called XRAM to enlarge the RAM space. It occupies the address space from 00H through FFH. The 768 bytes of XRAM are indirectly accessed by move external instruction MOVX @DPTR or MOVX @Ri. (See the demo code below.) Note that the stack pointer cannot be located in any part of XRAM.

XRAM demo code:

```
MOV    R0,#23H             ;write #5AH to XRAM with address @23H
MOV    A,#5AH
MOVX   @R0,A
MOV    R1,#23H             ;read from XRAM with address @23H
MOVX   A,@R1
MOV    DPTR,#0023H         ;write #5BH to XRAM with address @0023H
MOV    A,#5BH
MOVX   @DPTR,A
MOV    DPTR,#0023H         ;read from XRAM with address @0023H
MOVX   A,@DPTR
```

5.4 Non-Volatile Data Storage

By applying IAP, any page of APROM or LDROM can be used as non-volatile data storage. For IAP details, please see Section 21. “In-Application-Programming (IAP)” on page 214.

6. SPECIAL FUNCTION REGISTER (SFR)

The N76E003 uses Special Function Registers (SFRs) to control and monitor peripherals and their modes. The SFRs reside in the register locations 80 to FFH and are accessed by direct addressing only. SFRs those end their addresses as 0H or 8H are bit-addressable. It is very useful in cases where user would like to modify a particular bit directly without changing other bits via bit-field instructions. All other SFRs are byte-addressable only. The N76E003 contains all the SFRs presenting in the standard 8051. However some additional SFRs are built in. Therefore, some of unused bytes in the original 8051 have been given new functions. The SFRs are listed below.

To accommodate more than 128 SFRs in the 0x80 to 0xFF address space, SFR paging has been implemented. By default, all SFR accesses target SFR page 0. During device initialization, some SFRs located on SFR page 1 may need to be accessed. The register SFRS is used to switch SFR addressing page. Note that this register has TA write protection. Most of SFRs are available on both SFR page 0 and 1.

SFRS – SFR Page Selection (TA protected)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SFRPAGE
-	-	-	-	-	-	-	R/W

Address: 91H Reset value: 0000 0000b

Bit	Name	Description
0	SFRPAGE	**SFR page select** 0 = Instructions access SFR page 0. 1 = Instructions access SFR page 1.

Switch SFR page demo code:

```
MOV     TA,#0AAH            ;switch to SFR page 1
MOV     TA,#55H
ORL     SFRS,#01H

MOV     TA,#0AAH            ;switch to SFR page 0
MOV     TA,#55H
ANL     SFRS,#0FEH
```

Table 6-1. SFR Memory Map

SFR Page	Addr	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0 1	F8	SCON_1	PDTEN	PDTCNT	PMEN	PMD	PORDIS -	EIP1 -	EIPH1 -
0 1	F0	B	CAPCON3	CAPCON4	SPCR SPCR2	SPSR	SPDR -	AINDIDS -	EIPH -
0 1	E8	ADCCON0	PICON	PINEN	PIPEN	PIF	C2L	C2H	EIP -
0 1	E0	ACC	ADCCON1	ADCCON2	ADCDLY	C0L	C0H	C1L	C1H
0 1	D8	PWMCON0	PWMPL	PWM0L	PWM1L	PWM2L	PWM3L	PIOCON0	PWMCON1
0 1	D0	PSW	PWMPH	PWM0H	PWM1H	PWM2H	PWM3H	PNP	FBD
0 1	C8	T2CON	T2MOD	RCMP2L	RCMP2H	TL2 PWM4L	TH2 PWM5L	ADCMPL	ADCMPH
0 1	C0	I2CON	I2ADDR	ADCRL	ADCRH	T3CON PWM4H	RL3 PWM5H	RH3 PIOCON1	TA
0 1	B8	IP	SADEN	SADEN_1	SADDR_1	I2DAT	I2STAT	I2CLK	I2TOC
0 1	B0	P3	P0M1 P0S	P0M2 P0SR	P1M1 P1S	P1M2 P1SR	P2S	-	IPH PWMINTC
0 1	A8	IE	SADDR	WDCON	BODCON1	P3M1 P3S	P3M2 P3SR	IAPFD	IAPCN
0 1	A0	P2	-	AUXR1	BODCON0	IAPTRG	IAPUEN	IAPAL	IAPAH
0 1	98	SCON	SBUF	SBUF_1	EIE	EIE1	-	-	CHPCON
0 1	90	P1	SFRS	CAPCON0	CAPCON1	CAPCON2	CKDIV	CKSWT	CKEN
0 1	88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	WKCON
0 1	80	P0	SP	DPL	DPH	RCTRIM0	RCTRIM1	RWK	PCON

Unoccupied addresses in the SFR space marked in "-" are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided.

Table 6-2. SFR Definitions and Reset Values

Symbol	Definition	Address /(Page)	MSB							LSB[1]	Reset Value[2]
EIPH1	Extensive interrupt priority high 1	FFH/(0)	-	-	-	-	-	PWKTH	PT3H	PSH_1	0000 0000b
EIP1	Extensive interrupt priority 1	FEH/(0)	-	-	-	-	-	PWKT	PT3	PS_1	0000 0000b
PMD	PWM mask data	FCH	-	-	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000b
PMEN	PWM mask enable	FBH	-	-	PMEN5	PMEN4	PMEN3	PMEN2	PMEN1	PMEN0	0000 0000b
PDTCNT[4]	PWM dead-time counter	FAH	PDTCNT[7:0]								0000 0000b
PDTEN[4]	PWM dead-time enable	F9H	-	-	-	PDTCNT.8	-	PDT45EN	PDT23EN	PDT01EN	0000 0000b
SCON_1	Serial port 1 control	F8H	(FF) SM0_1/ FE_1	(FE) SM1_1	(FD) SM2_1	(FC) REN_1	(FB) TB8_1	(FA) RB8_1	(F9) TI_1	(F8) RI_1	0000 0000b
EIPH	Extensive interrupt priority high	F7H	PT2H	PSPIH	PFBH	PWDTH	PPWMH	PCAPH	PPIH	PI2CH	0000 0000b
AINDIDS	ADC channel digital input disable	F6H	P11DIDS	P03DIDS	P04DIDS	P05DIDS	P06DIDS	P07DIDS	P30DIDS	P17DIDS	0000 0000b
SPDR	SPI data	F5H(0)	SPDR[7:0]								0000 0000b
SPSR	SPI status	F4H	SPIF	WCOL	SPIOVF	MODF	DISMODF	-	-	-	0000 0000b
SPCR	SPI control	F3H(0)	SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR[1:0]		0000 0000b
SPCR2	SPI control 2	F3H(1)	-	-	-	-	-	-	SPIS[1:0]		0000 0000b
CAPCON4	Input capture control 4	F2H	-	-	-	-	CAP23	CAP22	CAP21	CAP20	0000 0000b
CAPCON3	Input capture control 3	F1H	CAP13	CAP12	CAP11	CAP10	CAP03	CAP02	CAP01	CAP00	0000 0000b
B	B register	F0H	(F7) B.7	(F6) B.6	(F5) B.5	(F4) B.4	(F3) B.3	(F2) B.2	(F1) B.1	(F0) B.0	0000 0000b
EIP	Extensive interrupt priority	EFH	PT2	PSPI	PFB	PWDT	PPWM	PCAP	PPI	PI2C	0000 0000b
C2H	Input capture 2 high byte	EEH	C2H[7:0]								0000 0000b
C2L	Input capture 2 low byte	EDH	C2L[7:0]								0000 0000b
PIF	Pin interrupt flag	ECH	PIF7	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	0000 0000b
PIPEN	Pin interrupt high level/rising edge enable	EBH	PIPEN7	PIPEN6	PIPEN5	PIPEN4	PIPEN3	PIPEN2	PIPEN1	PIPEN0	0000 0000b
PINEN	Pin interrupt low level/falling edge enable	EAH	PINEN7	PINEN6	PINEN5	PINEN4	PINEN3	PINEN2	PINEN1	PINEN0	0000 0000b
PICON	Pin interrupt control	E9H	PIT67	PIT45	PIT3	PIT2	PIT1	PIT0	PIPS[1:0]		0000 0000b
ADCCON0	ADC control 0	E8H	(EF) ADCF	(EE) ADCS	(ED) ETGSEL1	(EC) ETGSEL0	(EB) ADCHS3	(EA) ADCHS2	(E9) ADCHS1	(E8) ADCHS0	0000 0000b
C1H	Input capture 1 high byte	E7H	C1H[7:0]								0000 0000b
C1L	Input capture 1 low byte	E6H	C1L[7:0]								0000 0000b
C0H	Input capture 0 high byte	E5H	C0H[7:0]								0000 0000b
C0L	Input capture 0 low byte	E4H	C0L[7:0]								0000 0000b
ADCDLY	ADC trigger delay	E3H	ADCDLY[7:0]								0000 0000b
ADCCON2	ADC control 2	E2H	ADFBEN	ADCMPOP	ADCMPEN	ADCMPO	-	-	-	ADCDLY.8	0000 0000b
ADCCON1	ADC control 1	E1H	-	STADCPX	-	-	ETGTYP[1:0]		ADCEX	ADCEN	0000 0000b
ACC	Accumulator	E0H	(E7) ACC.7	(E6) ACC.6	(E5) ACC.5	(E4) ACC.4	(E3) ACC.3	(E2) ACC.2	(E1) ACC.1	(E0) ACC.0	0000 0000b
PWMCON1	PWM control 1	DFH	PWMMOD[1:0]		GP	PWMTYP	FBINEN	PWMDIV[2:0]			0000 0000b
PIOCON0	PWM I/O switch 0	DEH	-	-	PIO05	PIO04	PIO03	PIO02	PIO01	PIO00	0000 0000b
PWM3L	PWM3 duty low byte	DDH	PWM3[7:0]								0000 0000b
PWM2L	PWM2 duty low byte	DCH	PWM2[7:0]								0000 0000b
PWM1L	PWM1 duty low byte	DBH	PWM1[7:0]								0000 0000b
PWM0L	PWM0 duty low byte	DAH	PWM0[7:0]								0000 0000b
PWMPL	PWM period low byte	D9H	PWMP[7:0]								0000 0000b
PWMCON0	PWM control 0	D8H	(DF) PWMRUN	(DE) LOAD	(DD) PWMF	(DC) CLRPWM	(DB) -	(DA) -	(D9) -	(D8) -	0000 0000b
FBD	Brake data	D7H	FBF	FBINLS	FBD5	FBD4	FBD3	FBD2	FBD1	FBD0	0000 0000b
PNP	PWM negative polarity	D6H	-	-	PNP5	PNP4	PNP3	PNP2	PNP1	PNP0	0000 0000b
PWM3H	PWM3 duty high byte	D5H	PWM3[15:8]								0000 0000b
PWM2H	PWM2 duty high byte	D4H	PWM2[15:8]								0000 0000b
PWM1H	PWM1 duty high byte	D3H	PWM1[15:8]								0000 0000b
PWM0H	PWM0 duty high byte	D2H	PWM0[15:8]								0000 0000b
PWMPH	PWM period high byte	D1H	PWMP[15:8]								0000 0000b
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) -	(D0) P	0000 0000b
ADCMPH	ADC compare high byte	CFH	ADCMP[11:4]								0000 0000b
ADCMPL	ADC compare low byte	CEH	-	-	-	-	ADCMP[3:0]				0000 0000b
PWM5L	PWM5 duty low byte	CDH(1)	PWM5[7:0]								0000 0000b
TH2	Timer 2 high byte	CDH(0)	TH2[7:0]								0000 0000b
PWM4L	PWM4 duty low byte	CCH(1)	PWM4[7:0]								0000 0000b

Table 6-2. SFR Definitions and Reset Values

Symbol	Definition	Address /(Page)	MSB							LSB[1]	Reset Value[2]
TL2	Timer 2 low byte	CCH(0)	TL2[7:0]								0000 0000b
RCMP2H	Timer 2 compare high byte	CBH	RCMP2H[7:0]								0000 0000b
RCMP2L	Timer 2 compare low byte	CAH(0)	RCMP2L[7:0]								0000 0000b
T2MOD	Timer 2 mode	C9H	LDEN	T2DIV[2:0]			CAPCR	CMPCR	LDTS[1:0]		0000 0000b
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) -	(CD) -	(CC) -	(CB) -	(CA) TR2	(C9) -	(C8)	0000 0000b
TA	Timed access protection	C7H	TA[7:0]								0000 0000b
PIOCON1	PWM I/O switch 1	C6H(1)	-	-	PIO15	-	PIO13	PIO12	PIO11	-	0000 0000b
RH3	Timer 3 reload high byte	C6H(0)	RH3[7:0]								0000 0000b
PWM5H	PWM5 duty high byte	C5H(1)	PWM5[15:8]								0000 0000b
RL3	Timer 3 reload low byte	C5H(0)	RL3[7:0]								0000 0000b
PWM4H	PWM4 duty high byte	C4H(1)	PWM4[15:8]								0000 0000b
T3CON	Timer 3 control	C4H(0)	SMOD_1	SMOD0_1	BRCK	TF3	TR3	T3PS[2:0]			0000 0000b
ADCRH	ADC result high byte	C3H	ADCR[11:4]								0000 0000b
ADCRL	ADC result low byte	C2H	-	-	-	-	ADCR[3:0]				0000 0000b
I2ADDR	I²C own slave address	C1H	I2ADDR[7:1]							GC	0000 0000b
I2CON	I²C control	C0H	(C7) -	(C6) I2CEN	(C4) STA	(C4) STO	(C3) SI	(C2) AA	(C1) -	(C0) I2CPX	0000 0000b
I2TOC	I²C time-out counter	BFH	-	-	-	-	-	I2TOCEN	DIV	I2TOF	0000 0000b
I2CLK	I²C clock	BEH	I2CLK[7:0]								0000 1001b
I2STAT	I²C status	BDH	I2STAT[7:3]					0	0	0	1111 1000b
I2DAT	I²C data	BCH	I2DAT[7:0]								0000 0000b
SADDR_1	Slave 1 address	BBH	SADDR_1[7:0]								0000 0000b
SADEN_1	Slave 1 address mask	BAH	SADEN_1[7:0]								0000 0000b
SADEN	Slave 0 address mask	B9H	SADEN[7:0]								0000 0000b
IP	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBOD	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000b
PWMINTC	PWM Interrupt Control	B7H(1)	-	-	INTTYP1	INTTYP0	-	INTSEL2	INTSEL1	INTSEL0	0000 0000b
IPH	Interrupt priority high	B7H(0)	-	PADCH	PBODH	PSH	PT1H	PX1H	PT0H	PX0H	0000 0000b
P2S	P20 Setting and Timer0/1 Output Enable	B5H	P20UP	-	-	-	T1OE	T0OE	-	P2S.0	0000 0000b
P1SR	P1 slew rate	B4H/(1)	P1SR.7	P1SR.6	P1SR.5	P1SR.4	P1SR.3	P1SR.2	P1SR.1	P1SR.0	0000 0000b
P1M2	P1 mode select 2	B4H/(0)	P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	0000 0000b
P1S	P1 Schmitt trigger input	B3H/(1)	P1S.7	P1S.6	P1S.5	P1S.4	P1S.3	P1S.2	P1S.1	P1S.0	0000 0000b
P1M1	P1 mode select 1	B3H/(0)	P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	1111 1111b
P0SR	P0 slew rate	B2H/(1)	P0SR.7	P0SR.6	P0SR.5	P0SR.4	P0SR.3	P0SR.2	P0SR.1	P0SR.0	0000 0000b
P0M2	P0 mode select 2	B2H/(0)	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	0000 0000b
P0S	P0 Schmitt trigger input	B1H/(1)	P0S.7	P0S.6	P0S.5	P0S.4	P0S.3	P0S.2	P0S.1	P0S.0	0000 0000b
P0M1	P0 mode select 1	B1H/(0)	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	1111 1111b
P3	Port 3	B0H	(B7) 0	(B6) 0	(B5) 0	(B4) 0	(B3) 0	(B2) 0	(B1) 0	(B0) P3.0	Output latch, 0000 0001b Input, 0000 000Xb[3]
IAPCN	IAP control	AFH	IAPA[17:16]		FOEN	FCEN	FCTRL[3:0]				0011 0000b
IAPFD	IAP flash data	AEH	IAPFD[7:0]								0000 0000b
P3SR	P3 slew rate	ADH/(1)	-	-	-	-	-	-	-	P3SR.0	0000 0000b
P3M2	P3 mode select 2	ADH/(0)	-	-	-	-	-	-	-	P3M2.0	0000 0000b
P3S	P3 Schmitt trigger input	ACH/(1)	-	-	-	-	-	-	-	P3S.0	0000 0000b
P3M1	P3 mode select 1	ACH/(0)	-	-	-	-	-	-	-	P3M1.0	0000 0001b
BODCON1[4]	Brown-out detection control 1	ABH	-	-	-	-	-	LPBOD[1:0]		BODFLT	POR, 0000 0001b Others, 0000 0UUUb
WDCON[4]	Watchdog Timer control	AAH	WDTR	WDCLR	WDTF	WIDPD	WDTRF	WDPS[2:0]			POR, 0000 0111b WDT, 0000 1UUUb Others, 0000 UUUUb

Table 6-2. SFR Definitions and Reset Values

Symbol	Definition	Address /(Page)	MSB							LSB[1]	Reset Value[2]
SADDR	Slave 0 address	A9H	SADDR[7:0]								0000 0000b
IE	Interrupt enable	A8H	(AF) EA	(AE) EADC	(AD) EBOD	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000b
IAPAH	IAP address high byte	A7H	IAPA[15:8]								0000 0000b
IAPAL	IAP address low byte	A6H	IAPA[7:0]								0000 0000b
IAPUEN[4]	IAP update enable	A5H	-	-	-	-	-	CFUEN	LDUEN	APUEN	0000 0000b
IAPTRG[4]	IAP trigger	A4H	-	-	-	-	-	-	-	IAPGO	0000 0000b
BODCON0[4]	Brown-out detection control 0	A3H	BODEN[5]	-	BOV[1:0][5]		BOF[6]	BORST[5]	BORF	BOS[7]	POR, CCCC XC0Xb BOD, UUUU XU1Xb Others, UUUU XUUXb
AUXR1	Auxiliary register 1	A2H	SWRF	RSTPINF	HardF	-	GF2	UART0PX	0	DPS	POR, 0000 0000b Software, 1U00 0000b $\overline{\text{RST}}$ pin, U100 0000b Others, UUU0 0000b
P2	Port 2	A0H	(A7) 0	(A6) 0	(A5) 0	(A4) 0	(A3) 0	(A2) 0	(A1) 0	(A0) P2.0	Output latch, 0000 000Xb Input, 0000 000Xb[3]
CHPCON[4]	Chip control	9FH	SWRST	IAPFF	-	-	-	-	BS[5]	IAPEN	Software, 0000 00U0b Others, 0000 00C0b
EIE1	Extensive interrupt enable 1	9CH	-	-	-	-	-	EWKT	ET3	ES_1	0000 0000b
EIE	Extensive interrupt enable	9BH	ET2	ESPI	EFB	EWDT	EPWM	ECAP	EPI	EI2C	0000 0000b
SBUF_1	Serial port 1 data buffer	9AH	SBUF_1[7:0]								0000 0000b
SBUF	Serial port 0 data buffer	99H	SBUF[7:0]								0000 0000b
SCON	Serial port 0 control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000b
CKEN[4]	Clock enable	97H	EXTEN[1:0]		HIRCEN	-	-	-	-	CKSWTF	0011 0000b
CKSWT[4]	Clock switch	96H	-	-	HIRCST	-	ECLKST	OSC[1:0]		-	0011 0000b
CKDIV	Clock divider	95H	CKDIV[7:0]								0000 0000b
CAPCON2	Input capture control 2	94H	-	ENF2	ENF1	ENF0	-	-	-	-	0000 0000b
CAPCON1	Input capture control 1	93H	-	-	CAP2LS[1:0]		CAP1LS[1:0]		CAP0LS[1:0]		0000 0000b
CAPCON0	Input capture control 0	92H	-	CAPEN2	CAPEN1	CAPEN0	-	CAPF2	CAPF1	CAPF0	0000 0000b
SFRS[4]	SFR page selection	91H	-	-	-	-	-	-	-	SFRPSEL	0000 0000b
P1	Port 1	90H	(97) P1.7	(96) P1.6	(95) P1.5	(94) P1.4	(93) P1.3	(92) P1.2	(91) P1.1	(90) P1.0	Output latch, 1111 1111b Input, XXXX XXXXb[3]
WKCON	Self Wake-up Timer control	8FH	-	-	-	WKTF	WKTR	WKPS[2:0]			0000 0000b
CKCON	Clock control	8EH	-	PWMCKS	-	T1M	T0M	-	CLOEN	-	0000 0000b
TH1	Timer 1 high byte	8DH	TH1[7:0]								0000 0000b
TH0	Timer 0 high byte	8CH	TH0[7:0]								0000 0000b
TL1	Timer 1 low byte	8BH	TL1[7:0]								0000 0000b
TL0	Timer 0 low byte	8AH	TL0[7:0]								0000 0000b
TMOD	Timer 0 and 1 mode	89H	GATE	$\overline{\text{C/T}}$	M1	M0	GATE	$\overline{\text{C/T}}$	M1	M0	0000 0000b
TCON	Timer 0 and 1control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000b
PCON	Power control	87H	SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL	POR, 0001 0000b Others, 000U 0000b
RWK	Self Wake-up Timer reload byte	86H	RWK[7:0]								0000 0000b
RCTRIM1	Internal RC trim value low byte	85H	-	-	-	-	-	-	-	HIRCTRIM[0]	0000 0000b
RCTRIM0	Internal RC trim value	84H	HIRCTRIM[8:1]								0000 0000b

Table 6-2. SFR Definitions and Reset Values

Symbol	Definition	Address /(Page)	MSB							LSB[1]	Reset Value[2]
	high byte										
DPH	Data pointer high byte	83H	DPTR[15:8]								0000 0000b
DPL	Data pointer low byte	82H	DPTR[7:0]								0000 0000b
SP	Stack pointer	81H	SP[7:0]								0000 0111b
P0	Port 0	80H	(87) P0.7	(86) P0.6	(85) P0.5	(84) P0.4	(83) P0.3	(82) P0.2	(81) P0.1	(80) P0.0	Output latch, 1111 1111b Input, XXXX XXXXb[3]

[1] ( ) item means the bit address in bit-addressable SFRs.
[2] Reset value symbol description. 0: logic 0; 1: logic 1; U: unchanged; C: see [5]; X: see [3], [6], and [7].
[3] All I/O pins are default input-only mode (floating) after reset. Reading back P2.0 is always 0 if RPD (CONFIG0.2) remains un-programmed 1.
[4] These SFRs have TA protected writing.
[5] These SFRs have bits those are initialized according to CONFIG values after specified resets.
[6] BOF reset value depends on different setting of CONFIG2 and V_{DD} voltage level. Please check Table 24-1.
[7] BOS is a read-only flag decided by V_{DD} level while brown-out detection is enabled.

Bits marked in "-" are reserved for future use. They must be kept in their own initial states. Accessing these bits may cause an unpredictable effect.

6.1 ALL SFR DESCRIPTION

Following list all SFR description. For each SFR define also list in function IP chapter.

P0 – Port 0 (Bit-addressable)

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 80H Reset value: 1111 1111b

Bit	Name	Description
7:0	P0[7:0]	**Port 0** Port 0 is an maximum 8-bit general purpose I/O port.

SP – Stack Pointer

7	6	5	4	3	2	1	0
SP[7:0]							
R/W							

Address: 81H Reset value: 0000 0111b

Bit	Name	Description
7:0	SP[7:0]	**Stack pointer** The Stack Pointer stores the scratch-pad RAM address where the stack begins. It is incremented before data is stored during PUSH or CALL instructions. Note that the default value of SP is 07H. This causes the stack to begin at location 08H.

DPL – Data Pointer Low Byte

7	6	5	4	3	2	1	0
DPL[7:0]							
R/W							

Address: 82H Reset value: 0000 0000b

Bit	Name	Description
7:0	DPL[7:0]	**Data pointer low byte** This is the low byte of 16-bit data pointer. DPL combined with DPH serve as a 16-bit data pointer DPTR to access indirect addressed RAM or Program Memory. DPS (AUXR1.0) bit decides which data pointer, DPTR or DPTR1, is activated.

DPH – Data Pointer High Byte

7	6	5	4	3	2	1	0
DPH[7:0]							
R/W							

Address: 83H Reset value: 0000 0000b

Bit	Name	Description
7:0	DPH[7:0]	**Data pointer high byte** This is the high byte of 16-bit data pointer. DPH combined with DPL serve as a 16-bit data pointer DPTR to access indirect addressed RAM or Program Memory. DPS (AUXR1.0) bit decides which data pointer, DPTR or DPTR1, is activated.

RWK – Self Wake-up Timer Reload Byte

7	6	5	4	3	2	1	0
RWK[7:0]							
R/W							

Address: 86H Reset value: 0000 0000b

Bit	Name	Description
7:0	RWK[7:0]	**WKT reload byte** It holds the 8-bit reload value of WKT. Note that RWK should not be FFH if the pre-scale is 1/1 for implement limitation.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W

Address: 87H Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
7	SMOD	**Serial port 0 double baud rate enable** Setting this bit doubles the serial port baud rate when UART0 is in Mode 2 or when Timer 1 overflow is used as the baud rate source of UART0 Mode 1 or 3. See Table 13-1. Serial Port 0 Mode Description for details.
6	SMOD0	**Serial port 0 framing error flag access enable** 0 = SCON.7 accesses to SM0 bit. 1 = SCON.7 accesses to FE bit.

Bit	Name	Description
4	POF	**Power-on reset flag** This bit will be set as 1 after a power-on reset. It indicates a cold reset, a power-on reset complete. This bit remains its value after any other resets. This flag is recommended to be cleared via software.
3	GF1	**General purpose flag 1** The general purpose flag that can be set or cleared by user via software.
2	GF0	**General purpose flag 0** The general purpose flag that can be set or cleared by user via software.
1	PD	**Power-down mode** Setting this bit puts CPU into Power-down mode. Under this mode, both CPU and peripheral clocks stop and Program Counter (PC) suspends. It provides the lowest power consumption. After CPU is woken up from Power-down, this bit will be automatically cleared via hardware and the program continue executing the interrupt service routine (ISR) of the very interrupt source that woke the system up before. After return from the ISR, the device continues execution at the instruction, which follows the instruction that put the system into Power-down mode. Note that If IDL bit and PD bit are set simultaneously, CPU will enter Power-down mode. Then it does not go to Idle mode after exiting Power-down.
0	IDL	**Idle mode** Setting this bit puts CPU into Idle mode. Under this mode, the CPU clock stops and Program Counter (PC) suspends but all peripherals keep activated. After CPU is woken up from Idle, this bit will be automatically cleared via hardware and the program continue executing the ISR of the very interrupt source that woke the system up before. After return from the ISR, the device continues execution at the instruction which follows the instruction that put the system into Idle mode.

TCON – Timer 0 and 1 Control (Bit-addressable)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R (level) R/W (edge)	R/W	R (level) R/W (edge)	R/W

Address: 88H Reset value: 0000 0000b

Bit	Name	Description
7	TF1	**Timer 1 overflow flag** This bit is set when Timer 1 overflows. It is automatically cleared by hardware when the program executes the Timer 1 interrupt service routine. This bit can be set or cleared by software.
6	TR1	**Timer 1 run control** 0 = Timer 1 Disabled. Clearing this bit will halt Timer 1 and the current count will be preserved in TH1 and TL1. 1 = Timer 1 Enabled.
5	TF0	**Timer 0 overflow flag** This bit is set when Timer 0 overflows. It is automatically cleared via hardware when the program executes the Timer 0 interrupt service routine. This bit can be set or cleared by software.
4	TR0	**Timer 0 run control** 0 = Timer 0 Disabled. Clearing this bit will halt Timer 0 and the current count will be preserved in TH0 and TL0. 1 = Timer 0 Enabled.

Bit	Name	Description
3	IE1	**External interrupt 1 edge flag** If IT1 = 1 (falling edge trigger), this flag will be set by hardware when a falling edge is detected. It remain set until cleared via software or cleared by hardware in the beginning of its interrupt service routine. If IT1 = 0 (low level trigger), this flag follows the inverse of the $\overline{\text{INT1}}$ input signal's logic level. Software cannot control it.
2	IT1	**External interrupt 1 type select** This bit selects by which type that $\overline{\text{INT1}}$ is triggered. 0 = $\overline{\text{INT1}}$ is low level triggered. 1 = $\overline{\text{INT1}}$ is falling edge triggered.
1	IE0	**External interrupt 0 edge flag** If IT0 = 1 (falling edge trigger), this flag will be set by hardware when a falling edge is detected. It remain set until cleared via software or cleared by hardware in the beginning of its interrupt service routine. If IT0 = 0 (low level trigger), this flag follows the inverse of the $\overline{\text{INT0}}$ input signal's logic level. Software cannot control it.
0	IT0	**External interrupt 0 type select** This bit selects by which type that $\overline{\text{INT0}}$ is triggered. 0 = $\overline{\text{INT0}}$ is low level triggered. 1 = $\overline{\text{INT0}}$ is falling edge triggered.

TMOD – Timer 0 and 1 Mode

7	6	5	4	3	2	1	0
GATE	$\overline{\text{C/T1}}$	M1	M0	GATE	$\overline{\text{C/T0}}$	M1	M0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 89H Reset value: 0000 0000b

Bit	Name	Description
7	GATE	**Timer 1 gate control** 0 = Timer 1 will clock when TR1 is 1 regardless of $\overline{\text{INT1}}$ logic level. 1 = Timer 1 will clock only when TR1 is 1 and $\overline{\text{INT1}}$ is logic 1.
6	$\overline{\text{C/T1}}$	**Timer 1 Counter/Timer select** 0 = Timer 1 is incremented by internal system clock. 1 = Timer 1 is incremented by the falling edge of the external pin T1.
5 4	M1 M0	**Timer 1 mode select** M1 M0 Timer 1 Mode 0 0 Mode 0: 13-bit Timer/Counter 0 1 Mode 1: 16-bit Timer/Counter 1 0 Mode 2: 8-bit Timer/Counter with auto-reload from TH1 1 1 Mode 3: Timer 1 halted
3	GATE	**Timer 0 gate control** 0 = Timer 0 will clock when TR0 is 1 regardless of $\overline{\text{INT0}}$ logic level. 1 = Timer 0 will clock only when TR0 is 1 and $\overline{\text{INT0}}$ is logic 1.
2	$\overline{\text{C/T0}}$	**Timer 0 Counter/Timer select** 0 = Timer 0 is incremented by internal system clock. 1 = Timer 0 is incremented by the falling edge of the external pin T0.
1	M1	**Timer 0 mode select**

Bit	Name	Description
0	M0	M1 M0 Timer 0 Mode 0 0 Mode 0: 13-bit Timer/Counter 0 1 Mode 1: 16-bit Timer/Counter 1 0 Mode 2: 8-bit Timer/Counter with auto-reload from TH0 1 1 Mode 3: TL0 as a 8-bit Timer/Counter and TH0 as a 8-bit Timer

TL0 – Timer 0 Low Byte

7	6	5	4	3	2	1	0
TL0[7:0]							
R/W							

Address: 8AH Reset value: 0000 0000b

Bit	Name	Description
7:0	TL0[7:0]	**Timer 0 low byte** The TL0 register is the low byte of the 16-bit counting register of Timer 0.

TL1 – Timer 1 Low Byte

7	6	5	4	3	2	1	0
TL1[7:0]							
R/W							

Address: 8BH Reset value: 0000 0000b

Bit	Name	Description
7:0	TL1[7:0]	**Timer 1 low byte** The TL1 register is the low byte of the 16-bit counting register of Timer 1.

TH0 – Timer 0 High Byte

7	6	5	4	3	2	1	0
TH0[7:0]							
R/W							

Address: 8CH Reset value: 0000 0000b

Bit	Name	Description
7:0	TH0[7:0]	**Timer 0 high byte** The TH0 register is the high byte of the 16-bit counting register of Timer 0.

TH1 – Timer 1 High Byte

7	6	5	4	3	2	1	0
TH1[7:0]							
R/W							

Address: 8DH Reset value: 0000 0000b

Bit	Name	Description
7:0	TH1[7:0]	**Timer 1 high byte** The TH1 register is the high byte of the 16-bit counting register of Timer 1.

CKCON – Clock Control

7	6	5	4	3	2	1	0
-	PWMCKS	-	T1M	T0M	-	CLOEN	-
-	R/W	-	R/W	R/W	-	R/W	-

Address: 8EH Reset value: 0000 0000b

Bit	Name	Description
6	PWMCKS	**PWM clock source select** 0 = The clock source of PWM is the system clock F_{SYS}. 1 = The clock source of PWM is the overflow of Timer 1.
4	T1M	**Timer 1 clock mode select** 0 = The clock source of Timer 1 is the system clock divided by 12. It maintains standard 8051 compatibility. 1 = The clock source of Timer 1 is direct the system clock.
3	T0M	**Timer 0 clock mode select** 0 = The clock source of Timer 0 is the system clock divided by 12. It maintains standard 8051 compatibility. 1 = The clock source of Timer 0 is direct the system clock.
1	CLOEN	**System clock output enable** 0 = System clock output Disabled. 1 = System clock output Enabled from CLO pin (P1.1).

WKCON – Self Wake-up Timer Control

7	6	5	4	3	2	1	0
-	-	-	WKTF	WKTR	WKPS[2:0]		
-	-	-	R/W	R/W	R/W		

Address: 8FH Reset value: 0000 0000b

Bit	Name	Description
4	WKTF	**WKT overflow flag** This bit is set when WKT overflows. If the WKT interrupt and the global interrupt are enabled, setting this bit will make CPU execute WKT interrupt service routine. This bit is not automatically cleared via hardware and should be cleared via software.
3	WKTR	**WKT run control** 0 = WKT is halted. 1 = WKT starts running. Note that the reload register RWK can only be written when WKT is halted (WKTR bit is 0). If WKT is written while WKTR is 1, result is unpredictable.
2:0	WKPS[2:0]	**WKT pre-scalar** These bits determine the pre-scale of WKT clock. 000 = 1/1. 001 = 1/4. 010 = 1/16. 011 = 1/64. 100 = 1/256. 101 = 1/512. 110 = 1/1024. 111 = 1/2048.

P1 – Port 1 (Bit-addressable)

7	6	5	4	3	2	1	0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 90H Reset value: 1111 1111b

Bit	Name	Description
7:0	P1[7:0]	**Port 1** Port 1 is an maximum 8-bit general purpose I/O port.

SFRS – SFR Page Selection (TA protected)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SFRPAGE
-	-	-	-	-	-	-	R/W

Address: 91H Reset value: 0000 0000b

Bit	Name	Description
0	SFRPAGE	**SFR page select** 0 = Instructions access SFR page 0. 1 = Instructions access SFR page 1.

CAPCON0 – Input Capture Control 0

7	6	5	4	3	2	1	0
-	CAPEN2	CAPEN1	CAPEN0	-	CAPF2	CAPF1	CAPF0
-	R/W	R/W	R/W	-	R/W	R/W	R/W

Address: 92H Reset value: 0000 0000b

Bit	Name	Description
6	CAPEN2	**Input capture 2 enable** 0 = Input capture channel 2 Disabled. 1 = Input capture channel 2 Enabled.
5	CAPEN1	**Input capture 1 enable** 0 = Input capture channel 1 Disabled. 1 = Input capture channel 1 Enabled.
4	CAPEN0	**Input capture 0 enable** 0 = Input capture channel 0 Disabled. 1 = Input capture channel 0 Enabled.
2	CAPF2	**Input capture 2 flag** This bit is set by hardware if the determined edge of input capture 2 occurs. This bit should cleared by software.
1	CAPF1	**Input capture 1 flag** This bit is set by hardware if the determined edge of input capture 1 occurs. This bit should cleared by software.
0	CAPF0	**Input capture 0 flag** This bit is set by hardware if the determined edge of input capture 0 occurs. This bit should cleared by software.

CAPCON1 – Input Capture Control 1

7	6	5	4	3	2	1	0
-	-	CAP2LS[1:0]		CAP1LS[1:0]		CAP0LS[1:0]	
-	-	R/W		R/W		R/W	

Address: 93H Reset value: 0000 0000b

Bit	Name	Description
5:4	CAP2LS[1:0]	**Input capture 2 level select** 00 = Falling edge. 01 = Rising edge. 10 = Either Rising or falling edge. 11 = Reserved.
3:2	CAP1LS[1:0]	**Input capture 1 level select** 00 = Falling edge. 01 = Rising edge. 10 = Either Rising or falling edge. 11 = Reserved.
1:0	CAP0LS[1:0]	**Input capture 0 level select** 00 = Falling edge. 01 = Rising edge. 10 = Either Rising or falling edge. 11 = Reserved.

CAPCON2 – Input Capture Control 2

7	6	5	4	3	2	1	0
-	ENF2	ENF1	ENF0	-	-	-	-
-	R/W	R/W	R/W	-	-	-	-

Address: 94H Reset value: 0000 0000b

Bit	Name	Description
6	ENF2	**Enable noise filer on input capture 2** 0 = Noise filter on input capture channel 2 Disabled. 1 = Noise filter on input capture channel 2 Enabled.
5	ENF1	**Enable noise filer on input capture 1** 0 = Noise filter on input capture channel 1 Disabled. 1 = Noise filter on input capture channel 1 Enabled.
4	ENF0	**Enable noise filer on input capture 0** 0 = Noise filter on input capture channel 0 Disabled. 1 = Noise filter on input capture channel 0 Enabled.

CKDIV – Clock Divider

7	6	5	4	3	2	1	0
CKDIV[7:0]							
R/W							

Address: 95H Reset value: 0000 0000b

Bit	Name	Description
7:0	CKDIV[7:0]	**Clock divider** The system clock frequency F_{SYS} follows the equation below according to CKDIV value. $F_{SYS} = F_{OSC}$, while CKDIV = 00H, and $F_{SYS} = \frac{F_{OSC}}{2 \times CKDIV}$, while CKDIV = 01H to FFH.

CKSWT – Clock Switch (TA protected)

7	6	5	4	3	2	1	0
-	-	HIRCST	LIRCST	ECLKST	OSC[1:0]		-
-	-	R	R	R	W		-

Address: 96H Reset value: 0011 0000b

Bit	Name	Description
7	-	**Reserved**
6	-	**Reserved**
5	HIRCST	**High-speed internal oscillator 16 MHz status** 0 = High-speed internal oscillator is not stable or disabled. 1 = High-speed internal oscillator is enabled and stable.
-	-	**Reserved**
3	ECLKST	**External clock input status** 0 = External clock input is not stable or disabled. 1 = External clock input is enabled and stable.
2:1	OSC[1:0]	**Oscillator selection bits** This field selects the system clock source. 00 = Internal 16 MHz oscillator. 01 = External clock source according to EXTEN[1:0] (CKEN[7:6]) setting. 10 = Internal 10 kHz oscillator. 11 = Reserved. Note that this field is write only. The read back value of this field may not correspond to the present system clock source.

CKEN – Clock Enable (TA protected)

7	6	5	4	3	2	1	0
EXTEN[1:0]		HIRCEN	-	-	-	-	CKSWTF
R/W		R/W	-	-	-	-	R

Address: 97H Reset value: 0011 0000b

Bit	Name	Description
7:6	EXTEN[1:0]	**External clock source enable** 11 = External clock input via XIN Enabled. Others = external clock input is disable. P30 work as general purpose I/O.
5	HIRCEN	**High-speed internal oscillator 16 MHz enable** 0 = The high-speed internal oscillator Disabled. 1 = The high-speed internal oscillator Enabled. Note that once IAP is enabled by setting IAPEN (CHPCON.0), the high-speed internal 16 MHz oscillator will be enabled automatically. The hardware will also set HIRCEN and HIRCST bits. After IAPEN is cleared, HIRCEN and EHRCST resume the original values.
4:1	-	**Reserved**
0	CKSWTF	**Clock switch fault flag** 0 = The previous system clock source switch was successful. 1 = User tried to switch to an instable or disabled clock source at the previous system clock source switch. If switching to an instable clock source, this bit remains 1 until the clock source is stable and switching is successful.

SCON – Serial Port Control (Bit-addressable)

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 98H Reset value: 0000 0000b

Bit	Name	Description
7	SM0/FE	**Serial port mode select**
6	SM1	SMOD0 (PCON.6) = 0: See Table 13-1. Serial Port 0 Mode Description for details. SMOD0 (PCON.6) = 1: SM0/FE bit is used as frame error (FE) status flag. It is cleared by software. 0 = Frame error (FE) did not occur. 1 = Frame error (FE) occurred and detected.

Bit	Name	Description
5	SM2	**Multiprocessor communication mode enable** The function of this bit is dependent on the serial port 0 mode. Mode 0: This bit select the baud rate between F_{SYS}/12 and F_{SYS}/2. 0 = The clock runs at F_{SYS}/12 baud rate. It maintains standard 8051 compatibility. 1 = The clock runs at F_{SYS}/2 baud rate for faster serial communication. Mode 1: This bit checks valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is valid only when the received stop bit is logic 1 and the received data matches “Given” or “Broadcast” address. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is valid only when the received 9th bit is logic 1 and the received data matches “Given” or “Broadcast” address.
4	REN	**Receiving enable** 0 = Serial port 0 reception Disabled. 1 = Serial port 0 reception Enabled in Mode 1,2, or 3. In Mode 0, reception is initiated by the condition REN = 1 and RI = 0.
3	TB8	**9th transmitted bit** This bit defines the state of the 9th transmission bit in serial port 0 Mode 2 or 3. It is not used in Mode 0 or 1.
2	RB8	**9th received bit** The bit identifies the logic level of the 9th received bit in serial port 0 Mode 2 or 3. In Mode 1, RB8 is the logic level of the received stop bit. SM2 bit as logic 1 has restriction for exception. RB8 is not used in Mode 0.
1	TI	**Transmission interrupt flag** This flag is set by hardware when a data frame has been transmitted by the serial port 0 after the 8th bit in Mode 0 or the last data bit in other modes. When the serial port 0 interrupt is enabled, setting this bit causes the CPU to execute the serial port 0 interrupt service routine. This bit should be cleared manually via software.
0	RI	**Receiving interrupt flag** This flag is set via hardware when a data frame has been received by the serial port 0 after the 8th bit in Mode 0 or after sampling the stop bit in Mode 1, 2, or 3. SM2 bit as logic 1 has restriction for exception. When the serial port 0 interrupt is enabled, setting this bit causes the CPU to execute to the serial port 0 interrupt service routine. This bit should be cleared manually via software.

SBUF – Serial Port 0 Data Buffer

7	6	5	4	3	2	1	0
SBUF[7:0]							
R/W							

Address: 99H Reset value: 0000 0000b

Bit	Name	Description
7:0	SBUF[7:0]	**Serial port 0 data buffer** This byte actually consists two separate registers. One is the receiving resister, and the other is the transmitting buffer. When data is moved to SBUF, it goes to the transmitting buffer and is shifted for serial transmission. When data is moved from SBUF, it comes from the receiving register. The transmission is initiated through giving data to SBUF.

SBUF_1 – Serial Port 1 Data Buffer

7	6	5	4	3	2	1	0
SBUF_1[7:0]							
R/W							

Address: 9AH Reset value: 0000 0000b

Bit	Name	Description
7:0	SBUF_1[7:0]	**Serial port 1 data buffer** This byte actually consists two separate registers. One is the receiving resister, and the other is the transmitting buffer. When data is moved to SBUF_1, it goes to the transmitting buffer and is shifted for serial transmission. When data is moved from SBUF_1, it comes from the receiving register. The transmission is initiated through giving data to SBUF_1.

EIE – Extensive Interrupt Enable

7	6	5	4	3	2	1	0
ET2	ESPI	EFB	EWDT	EPWM	ECAP	EPI	EI2C
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 9BH Reset value: 0000 0000b

Bit	Name	Description
7	ET2	**Enable Timer 2 interrupt** 0 = Timer 2 interrupt Disabled. 1 = Interrupt generated by TF2 (T2CON.7) Enabled.
6	ESPI	**Enable SPI interrupt** 0 = SPI interrupt Disabled. 1 = Interrupt generated by SPIF (SPSR.7), SPIOVF (SPSR.5), or MODF (SPSR.4) Enable.
5	EFB	**Enable Fault Brake interrupt** 0 = Fault Brake interrupt Disabled. 1 = Interrupt generated by FBF (FBD.7) Enabled.
4	EWDT	**Enable WDT interrupt** 0 = WDT interrupt Disabled. 1 = Interrupt generated by WDTF (WDCON.5) Enabled.

Bit	Name	Description
3	EPWM	**Enable PWM interrupt** 0 = PWM interrupt Disabled. 1 = Interrupt generated by PWMF (PWMCON0.5) Enabled.
2	ECAP	**Enable input capture interrupt** 0 = Input capture interrupt Disabled. 1 = Interrupt generated by any flags of CAPF[2:0] (CAPCON0[2:0]) Enabled.
1	EPI	**Enable pin interrupt** 0 = Pin interrupt Disabled. 1 = Interrupt generated by any flags in PIF register Enabled.
0	EI2C	**Enable I^2C interrupt** 0 = I^2C interrupt Disabled. 1 = Interrupt generated by SI (I2CON.3) or I2TOF (I2TOC.0) Enabled.

EIE1 – Extensive Interrupt Enable 1

7	6	5	4	3	2	1	0
-	-	-	-	-	EWKT	ET3	ES_1
-	-	-	-	-	R/W	R/W	R/W

Address: 9CH Reset value: 0000 0000b

Bit	Name	Description
2	EWKT	**Enable WKT interrupt** 0 = WKT interrupt Disabled. 1 = Interrupt generated by WKTF (WKCON.4) Enabled.
1	ET3	**Enable Timer 3 interrupt** 0 = Timer 3 interrupt Disabled. 1 = Interrupt generated by TF3 (T3CON.4) Enabled.
0	ES_1	**Enable serial port 1 interrupt** 0 = Serial port 1 interrupt Disabled. 1 = Interrupt generated by TI_1 (SCON_1.1) or RI_1 (SCON_1.0) Enabled.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	IAPFF	-	-	-	-	BS	IAPEN
W	R/W	-	-	-	-	R/W	R/W

Address: 9FH Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
6	IAPFF	**IAP fault flag** The hardware will set this bit after IAPGO (ISPTRG.0) is set if any of the following condition is met: (1) The accessing address is oversize. (2) IAPCN command is invalid. (3) IAP erases or programs updating un-enabled block. (4) IAP erasing or programming operates under V_{BOD} while BOIAP (CONFIG2.5) remains un-programmed 1 with BODEN (BODCON0.7) as 1 and BORST (BODCON0.2) as 0. This bit should be cleared via software.
0	IAPEN	**IAP enable**

Bit	Name	Description
		0 = IAP function Disabled. 1 = IAP function Enabled. Once enabling IAP function, the HIRC will be turned on for timing control. To clear IAPEN should always be the last instruction after IAP operation to stop internal oscillator if reducing power consumption is concerned.
1	BS	**Boot select** This bit defines from which block that MCU re-boots after all resets. 0 = MCU will re-boot from APROM after all resets. 1 = MCU will re-boot from LDROM after all resets.
0	IAPEN	**IAP enable** 0 = IAP function Disabled. 1 = IAP function Enabled. Once enabling IAP function, the HIRC will be turned on for timing control. To clear IAPEN should always be the last instruction after IAP operation to stop internal oscillator if reducing power consumption is concerned.

P2 – Port 2 (Bit-addressable)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	P2.0
R	R	R	R	R	R	R	R

Address: A0H Reset value: 0000 000Xb

Bit	Name	Description
7:1	0	**Reserved** The bits are always read as 0.
0	P2.0	**Port 2 bit 0** P2.0 is an input-only pin when RPD (CONFIG0.2) is programmed as 0. When leaving RPD un-programmed, P2.0 is always read as 0.

AUXR1 – Auxiliary Register 1

7	6	5	4	3	2	1	0
SWRF	RSTPINF	HardF	-	GF2	UART0PX	0	DPS
R/W	R/W	R/W	-	R/W	R/W	R	R/W

Address: A2H Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
7	SWRF	**Software reset flag** When the MCU is reset via software reset, this bit will be set via hardware. It is recommended that the flag be cleared via software.
6	RSTPINF	**External reset flag** When the MCU is reset by the external reset pin, this bit will be set via hardware. It is recommended that the flag be cleared via software.
5	HardF	**Hard Fault reset flag** Once Program Counter (PC) is over flash size, MCU will be reset and this bit will be set via hardware. It is recommended that the flag be cleared via software. Note: If MCU run in OCD debug mode and OCDEN = 0, hard fault reset will be disabled and only HardF flag be asserted.

Bit	Name	Description
3	GF2	**General purpose flag 2** The general purpose flag that can be set or cleared by the user via software.
2	UART0PX	**Serial port 0 pin exchange** 0 = Assign RXD to P0.7 and TXD to P0.6 by default. 1 = Exchange RXD to P0.6 and TXD to P0.7. Note that TXD and RXD will exchange immediately once setting or clearing this bit. User should take care of not exchanging pins during transmission or receiving. Or it may cause unpredictable situation and no warning alarms.
1	0	**Reserved** This bit is always read as 0.
0	DPS	**Data pointer select** 0 = Data pointer 0 (DPTR) is active by default. 1 = Data pointer 1 (DPTR1) is active. After DPS switches the activated data pointer, the previous inactivated data pointer remains its original value unchanged.

BODCON0 – Brown-out Detection Control 0 (TA protected)

7	6	5	4	3	2	1	0
BODEN[1]		BOV[1:0][1]		BOF[2]	BORST[1]	BORF	BOS
R/W		R/W		R/W	R/W	R/W	R

Address: A3H Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
7	BODEN	**Brown-out detection enable** 0 = Brown-out detection circuit off. 1 = Brown-out detection circuit on. Note that BOD output is not available until 2~3 LIRC clocks after enabling.
6:4	BOV[1:0]	**Brown-out voltage select** 11 = V_{BOD} is 2.2V. 10 = V_{BOD} is 2.7V. 01 = V_{BOD} is 3.7V. 00 = V_{BOD} is 4.4V.
3	BOF	**Brown-out interrupt flag** This flag will be set as logic 1 via hardware after a V_{DD} dropping below or rising above V_{BOD} event occurs. If both EBOD (EIE.2) and EA (IE.7) are set, a brown-out interrupt requirement will be generated. This bit should be cleared via software.
2	BORST	**Brown-out reset enable** This bit decides whether a brown-out reset is caused by a power drop below V_{BOD}. 0 = Brown-out reset when V_{DD} drops below V_{BOD} Disabled. 1 = Brown-out reset when V_{DD} drops below V_{BOD} Enabled.
1	BORF	**Brown-out reset flag** When the MCU is reset by brown-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.
0	BOS	**Brown-out status** This bit indicates the V_{DD} voltage level comparing with V_{BOD} while BOD circuit is enabled. It keeps 0 if BOD is not enabled. 0 = V_{DD} voltage level is higher than V_{BOD} or BOD is disabled. 1 = V_{DD} voltage level is lower than V_{BOD}. Note that this bit is read-only.

[1] BODEN, BOV[1:0], and BORST are initialized by being directly loaded from CONFIG2 bit 7, [6:4], and 2 after all resets.

[2] BOF reset value depends on different setting of CONFIG2 and V_{DD} voltage level. Please check Table 24-1.

IAPTRG – IAP Trigger (TA protected)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	IAPGO
-	-	-	-	-	-	-	W

Address: A4H Reset value: 0000 0000b

Bit	Name	Description
0	IAPGO	**IAP go** IAP begins by setting this bit as logic 1. After this instruction, the CPU holds the Program Counter (PC) and the IAP hardware automation takes over to control the progress. After IAP action completed, the Program Counter continues to run the following instruction. The IAPGO bit will be automatically cleared and always read as logic 0. Before triggering an IAP action, interrupts (if enabled) should be temporary disabled for hardware limitation.

IAPUEN – IAP Updating Enable (TA protected)

7	6	5	4	3	2	1	0
-	-	-	-	-	CFUEN	LDUEN	APUEN
-	-	-	-	-	R/W	R/W	R/W

Address: A5H Reset value: 0000 0000b

Bit	Name	Description
2	CFUEN	**CONFIG bytes updated enable** 0 = Inhibit erasing or programming CONFIG bytes by IAP. 1 = Allow erasing or programming CONFIG bytes by IAP.
1	LDUEN	**LDROM updated enable** 0 = Inhibit erasing or programming LDROM by IAP. 1 = Allow erasing or programming LDROM by IAP.
0	APUEN	**APROM updated enable** 0 = Inhibit erasing or programming APROM by IAP. 1 = Allow erasing or programming APROM by IAP.

IAPAL – IAP Address Low Byte

7	6	5	4	3	2	1	0
IAPA[7:0]							
R/W							

Address: A6H Reset value: 0000 0000b

Bit	Name	Description
7:0	IAPA[7:0]	**IAP address low byte** IAPAL contains address IAPA[7:0] for IAP operations.

IAPAH – IAP Address High Byte

7	6	5	4	3	2	1	0
IAPA[15:8]							
R/W							

Address: A7H Reset value: 0000 0000b

Bit	Name	Description
7:0	IAPA[15:8]	**IAP address high byte** IAPAH contains address IAPA[15:8] for IAP operations.

IE – Interrupt Enable (Bit-addressable)

7	6	5	4	3	2	1	0
EA	EADC	EBOD	ES	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: A8H Reset value: 0000 0000b

Bit	Name	Description
7	EA	**Enable all interrupt** This bit globally enables/disables all interrupts that are individually enabled. 0 = All interrupt sources Disabled. 1 = Each interrupt Enabled depending on its individual mask setting. Individual interrupts will occur if enabled.
6	EADC	**Enable ADC interrupt** 0 = ADC interrupt Disabled. 1 = Interrupt generated by ADCF (ADCCON0.7) Enabled.
5	EBOD	**Enable brown-out interrupt** 0 = Brown-out detection interrupt Disabled. 1 = Interrupt generated by BOF (BODCON0.3) Enabled.
4	ES	**Enable serial port 0 interrupt** 0 = Serial port 0 interrupt Disabled. 1 = Interrupt generated by TI (SCON.1) or RI (SCON.0) Enabled.
3	ET1	**Enable Timer 1 interrupt** 0 = Timer 1 interrupt Disabled. 1 = Interrupt generated by TF1 (TCON.7) Enabled.
2	EX1	**Enable external interrupt 1** 0 = External interrupt 1 Disabled. 1 = Interrupt generated by $\overline{\text{INT1}}$ pin (P1.7) Enabled.
1	ET0	**Enable Timer 0 interrupt** 0 = Timer 0 interrupt Disabled. 1 = Interrupt generated by TF0 (TCON.5) Enabled.
0	EX0	**Enable external interrupt 0** 0 = External interrupt 0 Disabled. 1 = Interrupt generated by $\overline{\text{INT0}}$ pin (P3.0) Enabled.

SADDR – Slave 0 Address

7	6	5	4	3	2	1	0
SADDR[7:0]							
R/W							

Address: A9H Reset value: 0000 0000b

Bit	Name	Description
7:0	SADDR[7:0]	**Slave 0 address** his byte specifies the microcontroller's own slave address for UATR0 multi-processor communication.

WDCON – Watchdog Timer Control (TA protected)

7	6	5	4	3	2	1	0
WDTR	WDCLR	WDTF	WIDPD	WDTRF	WDPS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: AAH Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
7	WDTR	**WDT run** This bit is valid only when control bits in WDTEN[3:0] (CONFIG4[7:4]) are all 1. At this time, WDT works as a general purpose timer. 0 = WDT Disabled. 1 = WDT Enabled. The WDT counter starts running.
6	WDCLR	**WDT clear** Setting this bit will reset the WDT count to 00H. It puts the counter in a known state and prohibit the system from unpredictable reset. The meaning of writing and reading WDCLR bit is different. Writing: 0 = No effect. 1 = Clearing WDT counter. Reading: 0 = WDT counter is completely cleared. 1 = WDT counter is not yet cleared.
5	WDTF	**WDT time-out flag** This bit indicates an overflow of WDT counter. This flag should be cleared by software.
4	WIDPD	**WDT running in Idle or Power-down mode** This bit is valid only when control bits in WDTEN[3:0] (CONFIG4[7:4]) are all 1. It decides whether WDT runs in Idle or Power-down mode when WDT works as a general purpose timer. 0 = WDT stops running during Idle or Power-down mode. 1 = WDT keeps running during Idle or Power-down mode.
3	WDTRF	**WDT reset flag** When the MCU is reset by WDT time-out event, this bit will be set via hardware. It is recommended that the flag be cleared via software.
2:0	WDPS[2:0]	**WDT clock pre-scalar select** These bits determine the pre-scale of WDT clock from 1/1 through 1/256. See Table 11-1. The default is the maximum pre-scale value.

[1] WDTRF will be cleared after power-on reset, be set after WDT reset, and remains unchanged after any other resets.
[2] WDPS[2:0] are all set after power-on reset and keep unchanged after any reset other than power-on reset.

BODCON1 – Brown-out Detection Control 1 (TA protected)

7	6	5	4	3	2	1	0
-	-	-	-	-	LPBOD[1:0]		BODFLT
-	-	-	-	-	R/W		R/W

Address: ABH Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
7:3	-	**Reserved**
2:1	LPBOD[1:0]	**Low power BOD enable** 00 = BOD normal mode. BOD circuit is always enabled. 01 = BOD low power mode 1 by turning on BOD circuit every 1.6 ms periodically. 10 = BOD low power mode 2 by turning on BOD circuit every 6.4 ms periodically. 11 = BOD low power mode 3 by turning on BOD circuit every 25.6 ms periodically.
0	BODFLT	**BOD filter control** BOD has a filter which counts 32 clocks of F_{SYS} to filter the power noise when MCU runs with HIRC, or ECLK as the system clock and BOD does not operates in its low power mode (LPBOD[1:0] = [0, 0]). In other conditions, the filter counts 2 clocks of LIRC. Note that when CPU is halted in Power-down mode. The BOD output is permanently filtered by 2 clocks of LIRC. The BOD filter avoids the power noise to trigger BOD event. This bit controls BOD filter enabled or disabled. 0 = BOD filter Disabled. 1 = BOD filter Enabled. (Power-on reset default value.)

P3M1 – Port 3 Mode Select 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3M1.0[3]
-	-	-	-	-	-	-	R/W

Address: ACH, Page: 0 Reset value: 0000 0001b

Bit	Name	Description
0	P3M1.0	**Port 3 mode select 1**

[3] P3M1 and P3M2 are used in combination to determine the I/O mode of each pin of P3. See Table 7-1. Configuration for Different I/O Modes.

P3S – Port 3 Schmitt Triggered Input

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3S.0
-	-	-	-	-	-	-	R/W

Address: ACH, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
0	P3S.0	**P3.0 Schmitt triggered input** 0 = TTL level input of P3.0. 1 = Schmitt triggered input of P3.0.

P3M2 – Port 3 Mode Select 2

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3M2.0[3]
-	-	-	-	-	-	-	R/W

Address: ADH, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
0	P3M2.0	**Port 3 mode select 2**

[3] P3M1 and P3M2 are used in combination to determine the I/O mode of each pin of P3. See Table 7-1. Configuration for Different I/O Modes.

P3SR – Port 3 Slew Rate

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3SR.0
-	-	-	-	-	-	-	R/W

Address: ADH, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
0	P3SR.0	**P3.n slew rate** 0 = P3.0 normal output slew rate. 1 = P3.0 high-speed output slew rate.

IAPFD – IAP Flash Data

7	6	5	4	3	2	1	0
IAPFD[7:0]							
R/W							

Address: AEH Reset value: 0000 0000b

Bit	Name	Description
7:0	IAPFD[7:0]	**IAP flash data** This byte contains flash data, which is read from or is going to be written to the Flash Memory. User should write data into IAPFD for program mode before triggering IAP processing and read data from IAPFD for read/verify mode after IAP processing is finished.

IAPCN – IAP Control

7	6	5	4	3	2	1	0
IAPB[1:0]		FOEN	FCEN	FCTRL[3:0]			
R/W		R/W	R/W	R/W			

Address: AFH Reset value: 0011 0000b

Bit	Name	Description
7:6	IAPB[1:0]	**IAP control** This byte is used for IAP command. For details, see Table 21-1. IAP Modes and Command Codes.
5	FOEN	
4	FCEN	
3:0	FCTRL[3:0]	

P3 – Port 3 (Bit-addressable)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	P3.0
R	R	R	R	R	R	R	R/W

Address: B0H Reset value: 0000 0001b

Bit	Name	Description
7:1	0	**Reserved** The bits are always read as 0.
0	P3.0	**Port 3 bit 0** P3.0 is available only when the internal oscillator is used as the system clock. At this moment, P3.0 functions as a general purpose I/O. If the system clock is not selected as the internal oscillator, P3.0 pin functions as OSCIN. A write to P3.0 is invalid and P3.0 is always read as 0.

P0M1 – Port 0 Mode Select 1[1]

7	6	5	4	3	2	1	0
P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B1H, Page: 0 Reset value: 1111 1111b

Bit	Name	Description
7:0	P0M1[7:0]	**Port 0 mode select 1**

[1] P0M1 and P0M2 are used in combination to determine the I/O mode of each pin of P0. See Table 7-1. Configuration for Different I/O Modes.

P0M1.n	P0M2.n	I/O Type
0	0	Quasi-bidirectional
0	1	Push-pull
1	0	Input-only (high-impedance)
1	1	Open-drain

P0S – Port 0 Schmitt Triggered Input

7	6	5	4	3	2	1	0
P0S.7	P0S.6	P0S.5	P0S.4	P0S.3	P0S.2	P0S.1	P0S.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B1H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
n	P0S.n	**P0.n Schmitt triggered input** 0 = TTL level input of P0.n. 1 = Schmitt triggered input of P0.n.

P0M2 – Port 0 Mode Select 2[1]

7	6	5	4	3	2	1	0
P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B2H, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
7:0	P0M2[7:0]	**Port 0 mode select 2**

[1] P0M1 and P0M2 are used in combination to determine the I/O mode of each pin of P0. See Table 7-1. Configuration for Different I/O Modes.

P0SR – Port 0 Slew Rate

7	6	5	4	3	2	1	0
P0SR.7	P0SR.6	P0SR.5	P0SR.4	P0SR.3	P0SR.2	P0SR.1	P0SR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B2H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
n	P0SR.n	**P0.n slew rate** 0 = P0.n normal output slew rate. 1 = P0.n high-speed output slew rate.

P1M1 – Port 1 Mode Select 1[2]

7	6	5	4	3	2	1	0
P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B3H, Page: 0 Reset value: 1111 1111b

Bit	Name	Description
7:0	P1M1[7:0]	**Port 1 mode select 1**

[2] P1M1 and P1M2 are used in combination to determine the I/O mode of each pin of P1. See Table 7-1. Configuration for Different I/O Modes.

P1S – Port 1 Schmitt Triggered Input

7	6	5	4	3	2	1	0
P1S.7	P1S.6	P1S.5	P1S.4	P1S.3	P1S.2	P1S.1	P1S.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B3H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
n	P1S.n	**P1.n Schmitt triggered input** 0 = TTL level input of P1.n. 1 = Schmitt triggered input of P1.n.

P1M2 – Port 1 Mode Select 2[2]

7	6	5	4	3	2	1	0
P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B4H, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
7:0	P1M2[7:0]	**Port 1 mode select 2.**

[2] P1M1 and P1M2 are used in combination to determine the I/O mode of each pin of P1. See Table 7-1. Configuration for Different I/O Modes.

P1SR – Port 1 Slew Rate

7	6	5	4	3	2	1	0
P1SR.7	P1SR.6	P1SR.5	P1SR.4	P1SR.3	P1SR.2	P1SR.1	P1SR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B4H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
n	P1SR.n	**P1.n slew rate** 0 = P1.n normal output slew rate. 1 = P1.n high-speed output slew rate.

P2S – P20 Setting and Timer01 Output Enable

7	6	5	4	3	2	1	0
P20UP	-	-	-	T1OE	T0OE	-	P2S.0
R/W	-	-	-	R/W	R/W	-	R/W

Address: B5H Reset value: 0000 0000b

Bit	Name	Description
7	P20UP	**P2.0 pull-up enable** 0 = P2.0 pull-up Disabled. 1 = P2.0 pull-up Enabled. This bit is valid only when RPD (CONFIG0.2) is programmed as 0. When selecting as a ___ pin, the pull-up is always enabled.
3	T1OE	**Timer 1 output enable** 0 = Timer 1 output Disabled. 1 = Timer 1 output Enabled from T1 pin. ot e that imer output should be enabled only when operating in its " imer" mode.
2	T0OE	**Timer 0 output enable** 0 = Timer 0 output Disabled. 1 = Timer 0 output Enabled from T0 pin. ot e that imer output should be enabled only when operating in its " imer" mode.
0	P2S.0	**P2.0 Schmitt triggered input** 0 = TTL level input of P2.0. 1 = Schmitt triggered input of P2.0.

IPH – Interrupt Priority High[2]

7	6	5	4	3	2	1	0
-	PADCH	PBODH	PSH	PT1H	PX1H	PT0H	PX0H
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B7H, Page0 Reset value: 0000 0000b

Bit	Name	Description
6	PADC	**ADC interrupt priority high bit**
5	PBOD	**Brown-out detection interrupt priority high bit**
4	PSH	**Serial port 0 interrupt priority high bit**
3	PT1H	**Timer 1 interrupt priority high bit**

Bit	Name	Description
2	PX1H	**External interrupt 1 priority high bit**
1	PT0H	**Timer 0 interrupt priority high bit**
0	PX0H	**External interrupt 0 priority high bit**

[2] IPH is used in combination with the IP respectively to determine the priority of each interrupt source. See Table 20-2. Interrupt Priority Level Setting for correct interrupt priority configuration.

PWMINTC – PWM Interrupt Control

7	6	5	4	3	2	1	0
-	-	INTTYP1	INTTYP0	-	INTSEL2	INTSEL1	INTSEL0
-	-	R/W	R/W	-	R/W	R/W	R/W

Address: B7H, Page:1 Reset value: 0000 0000b

Bit	Name	Description
5:4	INTTYP[1:0]	**PWM interrupt type select** These bit select PWM interrupt type. 00 = Falling edge on PWM0/1/2/3/4/5 pin. 01 = Rising edge on PWM0/1/2/3/4/5 pin. 10 = Central point of a PWM period. 11 = End point of a PWM period. Note that the central point interrupt or the end point interrupt is only available while PWM operates in center-aligned type.
2:0	INTSEL[2:0]	**PWM interrupt pair select** These bits select which PWM channel asserts PWM interrupt when PWM interrupt type is selected as falling or rising edge on PWM0/1/2/3/4/5 pin.. 000 = PWM0. 001 = PWM1. 010 = PWM2. 011 = PWM3. 100 = PWM4. 101 = PWM5. Others = PWM0.

IP – Interrupt Priority (Bit-addressable)[1]

7	6	5	4	3	2	1	0
-	PADC	PBOD	PS	PT1	PX1	PT0	PX0
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B8H Reset value: 0000 0000b

Bit	Name	Description
6	PADC	**ADC interrupt priority low bit**
5	PBOD	**Brown-out detection interrupt priority low bit**
4	PS	**Serial port 0 interrupt priority low bit**
3	PT1	**Timer 1 interrupt priority low bit**
2	PX1	**External interrupt 1 priority low bit**
1	PT0	**Timer 0 interrupt priority low bit**
0	PX0	**External interrupt 0 priority low bit**

[1] IP is used in combination with the IPH to determine the priority of each interrupt source. See Table 20-2. Interrupt Priority Level Setting for correct interrupt priority configuration.

SADEN – Slave 0 Address Mask

7	6	5	4	3	2	1	0
SADEN[7:0]							
R/W							

Address: B9H Reset value: 0000 0000b

Bit	Name	Description
7:0	SADEN[7:0]	**Slave 0 address mask** This byte is a mask byte of UART0 that contains “don’t-care” bits (defined by zeros) to form the device’s “Given” address. The don’t-care bits provide the flexibility to address one or more slaves at a time.

SADEN_1 – Slave 1 Address Mask

7	6	5	4	3	2	1	0
SADEN_1[7:0]							
R/W							

Address: BAH Reset value: 0000 0000b

Bit	Name	Description
7:0	SADEN_1[7:0]	**Slave 1 address mask** This byte is a mask byte of UART1 that contains “don’t-care” bits (defined by zeros) to form the device’s “Given” address. The don’t-care bits provide the flexibility to address one or more slaves at a time.

SADDR_1 – Slave 1 Address

7	6	5	4	3	2	1	0
SADDR_1[7:0]							
R/W							

Address: BBH Reset value: 0000 0000b

Bit	Name	Description
7:0	SADDR_1[7:0]	**Slave 1 address** his byte specifies the microcontroller’s own slave address for UART1 multi-processor communication.

I2DAT – I²C Data

7	6	5	4	3	2	1	0
I2DAT[7:0]							
R/W							

Address: BCH Reset value: 0000 0000b

Bit	Name	Description
7:0	I2DAT[7:0]	**I²C data** I2DAT contains a byte of the I²C data to be transmitted or a byte, which has just received. Data in I2DAT remains as long as SI is logic 1. The result of reading or writing I2DAT during I²C transceiving progress is unpredicted. While data in I2DAT is shifted out, data on the bus is simultaneously being shifted in to update I2DAT. I2DAT always shows the last byte that presented on the I²C bus. Thus the event of lost arbitration, the original value of I2DAT changes after the transaction.

I2STAT – I²C Status

7	6	5	4	3	2	1	0
I2STAT[7:3]					0	0	0
R					R	R	R

Address: BDH Reset value: 1111 1000b

Bit	Name	Description
7:3	I2STAT[7:3]	**I²C status code** The MSB five bits of I2STAT contains the status code. There are 27 possible status codes. When I2STAT is F8H, no relevant state information is available and SI flag keeps 0. All other 26 status codes correspond to the I²C states. When each of these status is entered, SI will be set as logic 1 and a interrupt is requested.
2:0	0	**Reserved** The least significant three bits of I2STAT are always read as 0.

I2CLK – I²C Clock

7	6	5	4	3	2	1	0
I2CLK[7:0]							
R/W							

Address: BEH Reset value: 0000 1001b

Bit	Name	Description
7:0	I2CLK[7:0]	**I²C clock setting** In master mode: This register determines the clock rate of I²C bus when the device is in a master mode. The clock rate follows the equation, $\frac{F_{SYS}}{4 \times (I2CLK + 1)}$. The default value will make the clock rate of I²C bus 400k bps if the peripheral clock is 16 MHz. Note that the I2CLK value of 00H and 01H are not valid. This is an implement limitation. In slave mode: This byte has no effect. In slave mode, the I²C device will automatically synchronize with any given clock rate up to 400k bps.

I2TOC – I²C Time-out Counter

7	6	5	4	3	2	1	0
-	-	-	-	-	I2TOCEN	DIV	I2TOF
-	-	-	-	-	R/W	R/W	R/W

Address: BFH Reset value: 0000 0000b

Bit	Name	Description
2	I2TOCEN	**I²C time-out counter enable** 0 = I²C time-out counter Disabled. 1 = I²C time-out counter Enabled.
1	DIV	**I²C time-out counter clock divider** 0 = The clock of I²C time-out counter is F_{SYS}/1. 1 = The clock of I²C time-out counter is F_{SYS}/4.
0	I2TOF	**I²C time-out flag** This flag is set by hardware if 14-bit I²C time-out counter overflows. It is cleared by software.

I2CON – I²C Control (Bit-addressable)

7	6	5	4	3	2	1	0
-	I2CEN	STA	STO	SI	AA	-	I2CPX
-	R/W	R/W	R/W	R/W	R/W	-	R/W

Address: C0H Reset value: 0000 0000b

Bit	Name	Description
6	I2CEN	**I²C bus enable** 0 = I²C bus Disabled. 1 = I²C bus Enabled. Before enabling the I²C, SCL and SDA port latches should be set to logic 1.
5	STA	**START flag** When STA is set, the I²C generates a START condition if the bus is free. If the bus is busy, the I²C waits for a STOP condition and generates a START condition following. If STA is set while the I²C is already in the master mode and one or more bytes have been transmitted or received, the I²C generates a repeated START condition. Note that STA can be set anytime even in a slave mode, but STA is not hardware automatically cleared after START or repeated START condition has been detected. User should take care of it by clearing STA manually.
4	STO	**STOP flag** When STO is set if the I²C is in the master mode, a STOP condition is transmitted to the bus. STO is automatically cleared by hardware once the STOP condition has been detected on the bus. The STO flag setting is also used to recover the I²C device from the bus error state (I2STAT as 00H). In this case, no STOP condition is transmitted to the I²C bus. If the STA and STO bits are both set and the device is original in the master mode, the I²C bus will generate a STOP condition and immediately follow a START condition. If the device is in slave mode, STA and STO simultaneous setting should be avoid from issuing illegal I²C frames.
3	SI	**I²C interrupt flag** SI flag is set by hardware when one of 26 possible I²C status (besides F8H status) is entered. After SI is set, the software should read I2STAT register to determine which step has been passed and take actions for next step. SI is cleared by software. Before the SI is cleared, the low period of SCL line is stretched. The transaction is suspended. It is useful for the slave device to deal with previous data bytes until ready for receiving the next byte. The serial transaction is suspended until SI is cleared by software. After SI is cleared, I²C bus will continue to generate START or repeated START condition, STOP condition, 8-bit data, or so on depending on the software configuration of controlling byte or bits. Therefore, user should take care of it by preparing suitable setting of registers before SI is software cleared.

Bit	Name	Description
2	AA	**Acknowledge assert flag** If the AA flag is set, an ACK (low level on SDA) will be returned during the acknowledge clock pulse of the SCL line while the I²C device is a receiver or an own-address-matching slave. If the AA flag is cleared, a NACK (high level on SDA) will be returned during the acknowledge clock pulse of the SCL line while the I²C device is a receiver or an own-address-matching slave. A device with its own AA flag cleared will ignore its own salve address and the General Call. Consequently, SI will note be asserted and no interrupt is requested. Note that if an addressed slave does not return an ACK under slave receiver mode or not receive an ACK under slave transmitter mode, the slave device will become a not addressed slave. It cannot receive any data until its AA flag is set and a master addresses it again. There is a special case of I2STAT value C8H occurs under slave transmitter mode. Before the slave device transmit the last data byte to the master, AA flag can be cleared as 0. Then after the last data byte transmitted, the slave device will actively switch to not addressed slave mode of disconnecting with the master. The further reading by the master will be all FFH.
0	I2CPX	**I2C pins select** 0 = Assign SCL to P1.3 and SDA to P1.4. 1 = Assign SCL to P0.2 and SDA to P1.6. Note that I2C pins will exchange immediately once setting or clearing this bit.

I2ADDR – I²C Own Slave Address

7	6	5	4	3	2	1	0
I2ADDR[7:1]							GC
R/W							R/W

Address: C1H Reset value: 0000 0000b

Bit	Name	Description
7:1	I2ADDR[7:1]	**I²C device's own slave address** In master mode: These bits have no effect. In slave mode: These 7 bits define the slave address of this I²C device by user. The master should address I²C device by sending the same address in the first byte data after a START or a repeated START condition. If the AA flag is set, this I²C device will acknowledge the master after receiving its own address and become an addressed slave. Otherwise, the addressing from the master will be ignored. Note that I2ADDR[7:1] should not remain its default value of all 0, because address 0x00 is reserved for General Call.
6	GC	**General Call bit** In master mode: This bit has no effect. In slave mode: 0 = The General Call is always ignored. 1 = The General Call is recognized if AA flag is 1; otherwise, it is ignored if AA is 0.

ADCRL – ADC Result Low Byte

7	6	5	4	3	2	1	0
-	-	-	-	ADCR[3:0]			
-	-	-	-	R			

Address: C2H Reset value: 0000 0000b

Bit	Name	Description
3:0	ADCR[3:0]	**ADC result low byte** The least significant 4 bits of the ADC result stored in this register.

ADCRH – ADC Result High Byte

7	6	5	4	3	2	1	0
ADCR[11:4]							
R							

Address: C3H Reset value: 0000 0000b

Bit	Name	Description
7:0	ADCR[11:4]	**ADC result high byte** The most significant 8 bits of the ADC result stored in this register.

T3CON – Timer 3 Control

7	6	5	4	3	2	1	0
SMOD_1	SMOD0_1	BRCK	TF3	TR3	T3PS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: C4H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7	SMOD_1	**Serial port 1 double baud rate enable** Setting this bit doubles the serial port baud rate when UART1 is in Mode 2. See Table 13-2. Serial Port 1 Mode Description for details.
6	SMOD0_1	**Serial port 1 framing error access enable** 0 = SCON_1.7 accesses to SM0_1 bit. 1 = SCON_1.7 accesses to FE_1 bit.
5	BRCK	**Serial port 0 baud rate clock source** This bit selects which Timer is used as the baud rate clock source when serial port 0 is in Mode 1 or 3. 0 = Timer 1. 1 = Timer 3.
4	TF3	**Timer 3 overflow flag** This bit is set when Timer 3 overflows. It is automatically cleared by hardware when the program executes the Timer 3 interrupt service routine. This bit can be set or cleared by software.
3	TR3	**Timer 3 run control** 0 = Timer 3 is halted. 1 = Timer 3 starts running. Note that the reload registers RH3 and RL3 can only be written when Timer 3 is halted (TR3 bit is 0). If any of RH3 or RL3 is written if TR3 is 1, result is unpredictable.

Bit	Name	Description
2:0	T3PS[2:0]	**Timer 3 pre-scalar** These bits determine the scale of the clock divider for Timer 3. 000 = 1/1. 001 = 1/2. 010 = 1/4. 011 = 1/8. 100 = 1/16. 101 = 1/32. 110 = 1/64. 111 = 1/128.

PWM4H – PWM4 Duty High Byte

7	6	5	4	3	2	1	0
PWM4[15:8]							
R/W							

Address: C4H, Page:1 reset value: 0000 0000b

Bit	Name	Description
7:0	PWM4[15:8]	**PWM4 duty high byte** This byte with PWM4L controls the duty of the output signal PG4 from PWM generator.

RL3 – Timer 3 Reload Low Byte

7	6	5	4	3	2	1	0
RL3[7:0]							
R/W							

Address: C5H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	RL3[7:0]	**Timer 3 reload low byte** It holds the low byte of the reload value of Timer 3.

PWM5H – PWM5 Duty High Byte

7	6	5	4	3	2	1	0
PWM5[15:8]							
R/W							

Address: C5H, Page:1 reset value: 0000 0000b

Bit	Name	Description
7:0	PWM5[15:8]	**PWM5 duty high byte** This byte with PWM5L controls the duty of the output signal PG5 from PWM generator.

RH3 – Timer 3 Reload High Byte

7	6	5	4	3	2	1	0
RH3[7:0]							
R/W							

Address: C6H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	RH3[7:0]	**Timer 3 reload high byte** It holds the high byte of the reload value of Time 3.

PIOCON1 – PWM or I/O Select

7	6	5	4	3	2	1	0
-	-	PIO15	-	PIO13	PIO12	PIO11	-
-	-	R/W	-	R/W	R/W	R/W	-

Address: C6H, Page:1 Reset value: 0000 0000b

Bit	Name	Description
5	PIO15	**P1.5/PWM5 pin function select** 0 = P1.5/PWM5 pin functions as P1.5. 1 = P1.5/PWM5 pin functions as PWM5 output.
3	PIO13	**P0.4/PWM3 pin function select** 0 = P0.4/PWM3 pin functions as P0.4. 1 = P0.4/PWM3 pin functions as PWM3 output.
2	PIO12	**P0.5/PWM2 pin function select** 0 = P0.5/PWM2 pin functions as P0.5. 1 = P0.5/PWM2 pin functions as PWM2 output.
1	PIO11	**P1.4/PWM1 pin function select** 0 = P1.4/PWM1 pin functions as P1.4. 1 = P1.4/PWM1 pin functions as PWM1 output.

TA – Timed Access

7	6	5	4	3	2	1	0
TA[7:0]							
W							

Address: C7H Reset value: 0000 0000b

Bit	Name	Description
7:0	TA[7:0]	**Timed access** The timed access register controls the access to protected SFRs. To access protected bits, user should first write AAH to the TA and immediately followed by a write of 55H to TA. After these two steps, a writing permission window is opened for 4 clock cycles during this period that user may write to protected SFRs.

T2CON – Timer 2 Control

7	6	5	4	3	2	1	0
TF2	-	-	-	-	TR2	-	$\overline{\text{——}}$
R/W	-	-	-	-	R/W	-	R/W

Address: C8H Reset value: 0000 0000b

Bit	Name	Description
7	TF2	**Timer 2 overflow flag** This bit is set when Timer 2 overflows or a compare match occurs. If the Timer 2 interrupt and the global interrupt are enable, setting this bit will make CPU execute Timer 2 interrupt service routine. This bit is not automatically cleared via hardware and should be cleared via software.
2	TR2	**Timer 2 run control** 0 = Timer 2 Disabled. Clearing this bit will halt Timer 2 and the current count will be preserved in TH2 and TL2. 1 = Timer 2 Enabled.
0	$\overline{\text{——}}$	**Timer 2 compare or auto-reload mode select** This bit selects Timer 2 functioning mode. 0 = Auto-reload mode. 1 = Compare mode.

T2MOD – Timer 2 Mode

7	6	5	4	3	2	1	0
LDEN	T2DIV[2:0]			CAPCR	CMPCR	LDTS[1:0]	
R/W	R/W			R/W	R/W	R/W	

Address: C9H Reset value: 0000 0000b

Bit	Name	Description
7	LDEN	**Enable auto-reload** 0 = Reloading RCMP2H and RCMP2L to TH2 and TL2 Disabled. 1 = Reloading RCMP2H and RCMP2L to TH2 and TL2 Enabled.
6:4	T2DIV[2:0]	**Timer 2 clock divider** 000 = Timer 2 clock divider is 1/1. 001 = Timer 2 clock divider is 1/4. 010 = Timer 2 clock divider is 1/16. 011 = Timer 2 clock divider is 1/32. 100 = Timer 2 clock divider is 1/64. 101 = Timer 2 clock divider is 1/128. 110 = Timer 2 clock divider is 1/256. 111 = Timer 2 clock divider is 1/512.
3	CAPCR	**Capture auto-clear** This bit is valid only under Timer 2 auto-reload mode. It enables hardware auto-clearing TH2 and TL2 counter registers after they have been transferred in to RCMP2H and RCMP2L while a capture event occurs. 0 = Timer 2 continues counting when a capture event occurs. 1 = Timer 2 value is auto-cleared as 0000H when a capture event occurs.
2	CMPCR	**Compare match auto-clear** This bit is valid only under Timer 2 compare mode. It enables hardware auto-clearing TH2 and TL2 counter registers after a compare match occurs. 0 = Timer 2 continues counting when a compare match occurs. 1 = Timer 2 value is auto-cleared as 0000H when a compare match occurs.

Bit	Name	Description
1:0	LDTS[1:0]	**Auto-reload trigger select** These bits select the reload trigger event. 00 = Reload when Timer 2 overflows. 01 = Reload when input capture 0 event occurs. 10 = Reload when input capture 1 event occurs. 11 = Reload when input capture 2 event occurs.

RCMP2L – Timer 2 Reload/Compare Low Byte

7	6	5	4	3	2	1	0
RCMP2L[7:0]							
R/W							

Address: CAH Reset value: 0000 0000b

Bit	Name	Description
7:0	RCMP2L[7:0]	**Timer 2 reload/compare low byte** This register stores the low byte of compare value when Timer 2 is configured in compare mode. Also it holds the low byte of the reload value in auto-reload mode.

RCMP2H – Timer 2 Reload/Compare High Byte

7	6	5	4	3	2	1	0
RCMP2H[7:0]							
R/W							

Address: CBH Reset value: 0000 0000b

Bit	Name	Description
7:0	RCMP2H[7:0]	**Timer 2 reload/compare high byte** This register stores the high byte of compare value when Timer 2 is configured in compare mode. Also it holds the high byte of the reload value in auto-reload mode.

TL2 – Timer 2 Low Byte

7	6	5	4	3	2	1	0
TL2[7:0]							
R/W							

Address: CCH, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	TL2[7:0]	**Timer 2 low byte** The TL2 register is the low byte of the 16-bit counting register of Timer 2.

PWM4L – PWM4 Duty Low Byte

7	6	5	4	3	2	1	0
PWM4[7:0]							
R/W							

Address: CCH, Page:1 reset value: 0000 0000b

Bit	Name	Description
7:0	PWM4[7:0]	**PWM4 duty low byte** This byte with PWM4H controls the duty of the output signal PG4 from PWM generator.

TH2 – Timer 2 High Byte

7	6	5	4	3	2	1	0
TH2[7:0]							
R/W							

Address: CDH, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	TH2[7:0]	**Timer 2 high byte** The TH2 register is the high byte of the 16-bit counting register of Timer 2.

PWM5L – PWM5 Duty Low Byte

7	6	5	4	3	2	1	0
PWM5[7:0]							
R/W							

Address: CDH, Page:1 reset value: 0000 0000b

Bit	Name	Description
7:0	PWM5[7:0]	**PWM5 duty low byte** This byte with PWM5H controls the duty of the output signal PG5 from PWM generator.

ADCMPL – ADC Compare Low Byte

7	6	5	4	3	2	1	0
-	-	-	-	ADCMP[3:0]			
-	-	-	-	W/R			

Address: CEH Reset value: 0000 0000b

Bit	Name	Description
3:0	ADCMP[3:0]	**ADC compare low byte** The least significant 4 bits of the ADC compare value stores in this register.

ADCMPH – ADC Compare High Byte

7	6	5	4	3	2	1	0
ADCMP[11:4]							
W/R							

Address: CFH Reset value: 0000 0000b

Bit	Name	Description
7:0	ADCMP[11:4]	**ADC compare high byte** The most significant 8 bits of the ADC compare value stores in this register.

PSW – Program Status Word (Bit-addressable)

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Address: D0H Reset value: 0000 0000b

Bit	Name	Description
7	CY	**Carry flag** For a adding or subtracting operation, CY will be set when the previous operation resulted in a carry-out from or a borrow-in to the Most Significant bit, otherwise cleared. If the previous operation is MUL or DIV, CY is always 0. CY is affected by DA A instruction, which indicates that if the original BCD sum is greater than 100. For a CJNE branch, CY will be set if the first unsigned integer value is less than the second one. Otherwise, CY will be cleared.
6	AC	**Auxiliary carry** Set when the previous operation resulted in a carry-out from or a borrow-in to the 4th bit of the low order nibble, otherwise cleared.
5	F0	**User flag 0** The general purpose flag that can be set or cleared by user.
4	RS1	**Register bank selection bits** These two bits select one of four banks in which R0 to R7 locate.
3	RS0	RS1 RS0 Register Bank RAM Address 0 0 0 00H to 07H 0 1 1 08H to 0FH 1 0 2 10H to 17H 1 1 3 18H to 1FH
2	OV	**Overflow flag** OV is used for a signed character operands. For a ADD or ADDC instruction, OV will be set if there is a carry out of bit 6 but not out of bit 7, or a carry out of bit 7 but not bit 6. Otherwise, OV is cleared. OV indicates a negative number produced as the sum of two positive operands or a positive sum from two negative operands. For a SUBB, OV is set if a borrow is needed into bit6 but not into bit 7, or into bit7 but not bit 6. Otherwise, OV is cleared. OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number. For a MUL, if the product is greater than 255 (00FFH), OV will be set. Otherwise, it is cleared. For a DIV, it is normally 0. However, if B had originally contained 00H, the values returned in A and B will be undefined. Meanwhile, the OV will be set.

Bit	Name	Description
1	F1	**User flag 1** The general purpose flag that can be set or cleared by user via software.
0	P	**Parity flag** Set to 1 to indicate an odd number of ones in the accumulator. Cleared for an even number of ones. It performs even parity check.

Table 6-3. Instructions That Affect Flag Settings

Instruction	CY	OV	AC	Instruction	CY	OV	AC
ADD	X[1]	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, /bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, /bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

[1] X indicates the modification depends on the result of the instruction.

PWMPH – PWM Period High Byte

7	6	5	4	3	2	1	0
PWMP[15:8]							
R/W							

Address: D1H reset value: 0000 0000b

Bit	Name	Description
7:0	PWMP[15:8]	**PWM period high byte** This byte with PWMPL controls the period of the PWM generator signal.

PWM0H – PWM0 Duty High Byte

7	6	5	4	3	2	1	0
PWM0[15:8]							
R/W							

Address: D2H reset value: 0000 0000b

Bit	Name	Description
7:0	PWM0[15:8]	**PWM0 duty high byte** This byte with PWM0L controls the duty of the output signal PG0 from PWM generator.

PWM1H – PWM1 Duty High Byte

7	6	5	4	3	2	1	0
PWM1[15:8]							
R/W							

Address: D3H reset value: 0000 0000b

Bit	Name	Description
7:0	PWM1[15:8]	**PWM1 duty high byte** This byte with PWM1L controls the duty of the output signal PG1 from PWM generator.

PWM2H – PWM2 Duty High Byte

7	6	5	4	3	2	1	0
PWM2[15:8]							
R/W							

Address: D4H reset value: 0000 0000b

Bit	Name	Description
7:0	PWM2[15:8]	**PWM2 duty high byte** This byte with PWM2L controls the duty of the output signal PG2 from PWM generator.

PWM3H – PWM3 Duty High Byte

7	6	5	4	3	2	1	0
PWM3[15:8]							
R/W							

Address: D5H reset value: 0000 0000b

Bit	Name	Description
7:0	PWM3[15:8]	**PWM3 duty high byte** This byte with PWM3L controls the duty of the output signal PG3 from PWM generator.

PNP – PWM Negative Polarity

7	6	5	4	3	2	1	0
-	-	PNP5	PNP4	PNP3	PNP2	PNP1	PNP0
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Address: D6H Reset value: 0000 0000b

Bit	Name	Description
n	PNPn	**PWMn negative polarity output enable** 0 = PWMn signal outputs directly on PWMn pin. 1 = PWMn signal outputs inversely on PWMn pin.

FBD – PWM Fault Brake Data

7	6	5	4	3	2	1	0
FBF	FBINLS	FBD5	FBD4	FBD3	FBD2	FBD1	FBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: D7H Reset value: 0000 0000b

Bit	Name	Description
7	FBF	**Fault Brake flag** This flag is set when FBINEN is set as 1 and FB pin detects an edge, which matches FBINLS (FBD.6) selection. This bit is cleared by software. After FBF is cleared, Fault Brake data output will not be released until PWMRUN (PWMCON0.7) is set.
6	FBINLS	**FB pin input level selection** 0 = Falling edge. 1 = Rising edge.
N	FBDn	**PWMn Fault Brake data** 0 = PWMn signal is overwritten by 0 once Fault Brake asserted. 1 = PWMn signal is overwritten by 1 once Fault Brake asserted.

PWMCON0 – PWM Control 0 (Bit-addressable)

7	6	5	4	3	2	1	0
PWMRUN	LOAD	PWMF	CLRPWM	-	-	-	-
R/W	R/W	R/W	R/W	-	-	-	-

Address: D8H Reset value: 0000 0000b

Bit	Name	Description
7	PWMRUN	**PWM run enable** 0 = PWM stays in idle. 1 = PWM starts running.
6	LOAD	**PWM new period and duty load** This bit is used to load period and duty control registers in their buffer if new period or duty value needs to be updated. The loading will act while a PWM period is completed. The new period and duty affected on the next PWM cycle. After the loading is complete, LOAD will be automatically cleared via hardware. The meaning of writing and reading LOAD bit is different. <u>Writing:</u> 0 = No effect. 1 = Load new period and duty in their buffers while a PWM period is completed. <u>Reading:</u> 0 = A loading of new period and duty is finished. 1 = A loading of new period and duty is not yet finished.
5	PWMF	**PWM flag** This flag is set according to definitions of INTSEL[2:0] and INTTYP[1:0] in PWMINTC. This bit is cleared by software.

Bit	Name	Description
4	CLRPWM	**Clear PWM counter** Setting this bit clears the value of PWM 16-bit counter for resetting to 0000H. After the counter value is cleared, CLRPWM will be automatically cleared via hardware. The meaning of writing and reading CLRPWM bit is different. Writing: 0 = No effect. 1 = Clearing PWM 16-bit counter. Reading: 0 = PWM 16-bit counter is completely cleared. 1 = PWM 16-bit counter is not yet cleared.

PWMPL – PWM Period Low Byte

7	6	5	4	3	2	1	0
PWMP[7:0]							
R/W							

Address: D9H reset value: 0000 0000b

Bit	Name	Description
7:0	PWMP[7:0]	**PWM period low byte** This byte with PWMPH controls the period of the PWM generator signal.

PWM0L – PWM0 Duty Low Byte

7	6	5	4	3	2	1	0
PWM0[7:0]							
R/W							

Address: DAH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM0[7:0]	**PWM0 duty low byte** This byte with PWM0H controls the duty of the output signal PG0 from PWM generator.

PWM1L – PWM/1 Duty Low Byte

7	6	5	4	3	2	1	0
PWM1[7:0]							
R/W							

Address: DBH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM1[7:0]	**PWM1 duty low byte** This byte with PWM1H controls the duty of the output signal PG1 from PWM generator.

PWM2L – PWM2 Duty Low Byte

7	6	5	4	3	2	1	0
PWM2[7:0]							
R/W							

Address: DCH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM2[7:0]	**PWM2 duty low byte** This byte with PWM2H controls the duty of the output signal PG2 from PWM generator.

PWM3L – PWM3 Duty Low Byte

7	6	5	4	3	2	1	0
PWM3[7:0]							
R/W							

Address: DDH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM3[7:0]	**PWM3 duty low byte** This byte with PWM3H controls the duty of the output signal PG3 from PWM generator.

PIOCON0 – PWM or I/O Select

7	6	5	4	3	2	1	0
-	-	PIO05	PIO04	PIO03	PIO02	PIO01	PIO00
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Address: DEH Reset value: 0000 0000b

Bit	Name	Description
5	PIO05	**P0.3/PWM5 pin function select** 0 = P0.3/PWM5 pin functions as P0.3. 1 = P0.3/PWM5 pin functions as PWM5 output.
4	PIO04	**P0.1/PWM4 pin function select** 0 = P0.1/PWM4 pin functions as P0.1. 1 = P0.1/PWM4 pin functions as PWM4 output.
3	PIO03	**P0.0/PWM3 pin function select** 0 = P0.0/PWM3 pin functions as P0.0. 1 = P0.0/PWM3 pin functions as PWM3 output.
2	PIO02	**P1.0/PWM2 pin function select** 0 = P1.0/PWM2 pin functions as P1.0. 1 = P1.0/PWM2 pin functions as PWM2 output.
1	PIO01	**P1.1/PWM1 pin function select** 0 = P1.1/PWM1 pin functions as P1.1. 1 = P1.1/PWM1 pin functions as PWM1 output.
0	PIO00	**P1.2/PWM0 pin function select** 0 = P1.2/PWM0 pin functions as P1.2. 1 = P1.2/PWM0 pin functions as PWM0 output.

PWMCON1 – PWM Control 1

7	6	5	4	3	2	1	0
PWMMOD[1:0]		GP	PWMTYP	FBINEN	PWMDIV[2:0]		
R/W		R/W	R/W	R/W	R/W		

Address: DFH Reset value: 0000 0000b

Bit	Name	Description
5	GP	**Group mode enable** This bit enables the group mode. If enabled, the duty of first three pairs of PWM are decided by PWM01H and PWM01L rather than their original duty control registers. 0 = Group mode Disabled. 1 = Group mode Enabled.
2:0	PWMDIV[2:0]	**PWM clock divider** This field decides the pre-scale of PWM clock source. 000 = 1/1. 001 = 1/2 010 = 1/4. 011 = 1/8. 100 = 1/16. 101 = 1/32. 110 = 1/64. 111 = 1/128.

A or ACC – Accumulator (Bit-addressable)

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: E0H Reset value: 0000 0000b

Bit	Name	Description
7:0	ACC[7:0]	**Accumulator** The A or ACC register is the standard 80C51 accumulator for arithmetic operation.

ADCCON1 – ADC Control 1

7	6	5	4	3	2	1	0
-	STADCPX	-	-	ETGTYP[1:0]		ADCEX	ADCEN
-	R/W	-	-	R/W		R/W	R/W

Address: E1H Reset value: 0000 0000b

Bit	Name	Description
6	STADCPX	**External start ADC trigger pin select** 0 = Assign STADC to P0.4. 1 = Assign STADC to P1.3. Note that STADC will exchange immediately once setting or clearing this bit.

Bit	Name	Description
3:2	ETGTYP[1:0]	**External trigger type select** When ADCEX (ADCCON1.1) is set, these bits select which condition triggers ADC conversion. 00 = Falling edge on PWM0/2/4 or STADC pin. 01 = Rising edge on PWM0/2/4 or STADC pin. 10 = Central point of a PWM period. 11 = End point of a PWM period. Note that the central point interrupt or the period point interrupt is only available for PWM center-aligned type.
1	ADCEX	**ADC external conversion trigger select** This bit select the methods of triggering an A/D conversion. 0 = A/D conversion is started only via setting ADCS bit. 1 = A/D conversion is started via setting ADCS bit or by external trigger source depending on ETGSEL[1:0] and ETGTYP[1:0]. Note that while ADCS is 1 (busy in converting), the ADC will ignore the following external trigger until ADCS is hardware cleared.
0	ADCEN	**ADC enable** 0 = ADC circuit off. 1 = ADC circuit on.

ADCCON2 – ADC Control 2

7	6	5	4	3	2	1	0
ADFBEN	ADCMPOP	ADCMPEN	ADCMPO	-	-	-	ADCDLY.8
R/W	R/W	R/W	R	-	-	-	R/W

Address: E2H Reset value: 0000 0000b

Bit	Name	Description
7	ADFBEN	**ADC compare result asserting Fault Brake enable** 0 = ADC asserting Fault Brake Disabled. 1 = ADC asserting Fault Brake Enabled. Fault Brake is asserted once its compare result ADCMPO is 1. Meanwhile, PWM channels output Fault Brake data. PWMRUN (PWMCON0.7) will also be automatically cleared by hardware. The PWM output resumes when PWMRUN is set again.
6	ADCMPOP	**ADC comparator output polarity** 0 = ADCMPO is 1 if ADCR[11:0] is greater than or equal to ADCMP[11:0]. 1 = ADCMPO is 1 if ADCR[11:0] is less than ADCMP[11:0].
5	ADCMPEN	**ADC result comparator enable** 0 = ADC result comparator Disabled. 1 = ADC result comparator Enabled.
4	ADCMPO	**ADC comparator output value** This bit is the output value of ADC result comparator based on the setting of ACMPOP. This bit updates after every A/D conversion complete.
0	ADCDLY.8	**ADC external trigger delay counter bit 8** See ADCDLY register.

ADCDLY – ADC Trigger Delay Counter

7	6	5	4	3	2	1	0
ADCDLY[7:0]							
R/W							

Address: E3H Reset value: 0000 0000b

Bit	Name	Description
7:0	ADCDLY[7:0]	**ADC external trigger delay counter low byte** This 8-bit field combined with ADCCON2.0 forms a 9-bit counter. This counter inserts a delay after detecting the external trigger. An A/D converting starts after this period of delay. External trigger delay time = $\frac{ADCDLY}{F_{ADC}}$. Note that this field is valid only when ADCEX (ADCCON1.1) is set. User should not modify ADCDLY during PWM run time if selecting PWM output as the external ADC trigger source.

C0L – Capture 0 Low Byte

7	6	5	4	3	2	1	0
C0L[7:0]							
R/W							

Address: E4H Reset value: 0000 0000b

Bit	Name	Description
7:0	C0L[7:0]	**Input capture 0 result low byte** The C0L register is the low byte of the 16-bit result captured by input capture 0.

C0H – Capture 0 High Byte

7	6	5	4	3	2	1	0
C0H[7:0]							
R/W							

Address: E5H Reset value: 0000 0000b

Bit	Name	Description
7:0	C0H[7:0]	**Input capture 0 result high byte** The C0H register is the high byte of the 16-bit result captured by input capture 0.

C1L – Capture 1 Low Byte

7	6	5	4	3	2	1	0
C1L[7:0]							
R/W							

Address: E6H Reset value: 0000 0000b

Bit	Name	Description
7:0	C1L[7:0]	**Input capture 1 result low byte** The C1L register is the low byte of the 16-bit result captured by input capture 1.

C1H – Capture 1 High Byte

7	6	5	4	3	2	1	0
C1H[7:0]							
R/W							

Address: E7H Reset value: 0000 0000b

Bit	Name	Description
7:0	C1H[7:0]	**Input capture 1 result high byte** The C1H register is the high byte of the 16-bit result captured by input capture 1.

ADCCON0 – ADC Control 0 (Bit-addressable)

7	6	5	4	3	2	1	0
ADCF	ADCS	ETGSEL1	ETGSEL0	ADCHS3	ADCHS2	ADCHS1	ADCHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: E8H Reset value: 0000 0000b

Bit	Name	Description
7	ADCF	**ADC flag** This flag is set when an A/D conversion is completed. The ADC result can be read. While this flag is 1, ADC cannot start a new converting. This bit is cleared by software.
6	ADCS	**A/D converting software start trigger** Setting this bit 1 triggers an A/D conversion. This bit remains logic 1 during A/D converting time and is automatically cleared via hardware right after conversion complete. The meaning of writing and reading ADCS bit is different. Writing: 0 = No effect. 1 = Start an A/D converting. Reading: 0 = ADC is in idle state. 1 = ADC is busy in converting.
5:4	ETGSEL[1:0]	**External trigger source select** When ADCEX (ADCCON1.1) is set, these bits select which pin output triggers ADC conversion. 00 = PWM0. 01 = PWM2. 10 = PWM4. 11 = STADC pin.
3:0	ADCHS[3:0]	**A/D converting channel select** This filed selects the activating analog input source of ADC. If ADCEN is 0, all inputs are disconnected. 0000 = AIN0. 0001 = AIN1. 0010 = AIN2. 0011 = AIN3. 0100 = AIN4. 0101 = AIN5. 0110 = AIN6. 0111 = AIN7 1000 = Internal band-gap voltage. Others = Reserved.

PICON – Pin Interrupt Control

7	6	5	4	3	2	1	0
PIT67	PIT45	PIT3	PIT2	PIT1	PIT0	PIPS[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address: E9H Reset value: 0000 0000b

Bit	Name	Description
7	PIT67	**Pin interrupt channel 6 and 7 type select** This bit selects which type that pin interrupt channel 6 and 7 is triggered. 0 = Level triggered. 1 = Edge triggered.
6	PIT45	**Pin interrupt channel 4 and 5 type select** This bit selects which type that pin interrupt channel 4 and 5 is triggered. 0 = Level triggered. 1 = Edge triggered.
5	PIT3	**Pin interrupt channel 3 type select** This bit selects which type that pin interrupt channel 3 is triggered. 0 = Level triggered. 1 = Edge triggered.
4	PIT2	**Pin interrupt channel 2 type select** This bit selects which type that pin interrupt channel 2 is triggered. 0 = Level triggered. 1 = Edge triggered.
3	PIT1	**Pin interrupt channel 1 type select** This bit selects which type that pin interrupt channel 1 is triggered. 0 = Level triggered. 1 = Edge triggered.
2	PIT0	**Pin interrupt channel 0 type select** This bit selects which type that pin interrupt channel 0 is triggered. 0 = Level triggered. 1 = Edge triggered.
1:0	PIPS[:0]	**Pin interrupt port select** This field selects which port is active as the 8-channel of pin interrupt. 00 = Port 0. 01 = Port 1. 10 = Port 2. 11 = Port 3.

PINEN – Pin Interrupt Negative Polarity Enable.

7	6	5	4	3	2	1	0
PINEN7	PINEN6	PINEN5	PINEN4	PINEN3	PINEN2	PINEN1	PINEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: EAH Reset value: 0000 0000b

Bit	Name	Description
n	PINENn	**Pin interrupt channel n negative polarity enable** This bit enables low-level/falling edge triggering pin interrupt channel n. The level or edge triggered selection depends on each control bit PITn in PICON. 0 = Low-level/falling edge detect Disabled. 1 = Low-level/falling edge detect Enabled.

PIPEN – Pin Interrupt Positive Polarity Enable.

7	6	5	4	3	2	1	0
PIPEN7	PIPEN6	PIPEN5	PIPEN4	PIPEN3	PIPEN2	PIPEN1	PIPEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: EBH Reset value: 0000 0000b

Bit	Name	Description
n	PIPENn	**Pin interrupt channel n positive polarity enable** This bit enables high-level/rising edge triggering pin interrupt channel n. The level or edge triggered selection depends on each control bit PITn in PICON. 0 = High-level/rising edge detect Disabled. 1 = High-level/rising edge detect Enabled.

PIF – Pin Interrupt Flags

7	6	5	4	3	2	1	0
PIF7	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0
R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)

Address: ECH Reset value: 0000 0000b

Bit	Name	Description
n	PIFn	**Pin interrupt channel n flag** If the edge trigger is selected, this flag will be set by hardware if the channel n of pin interrupt detects an enabled edge trigger. This flag should be cleared by software. If the level trigger is selected, this flag follows the inverse of the input signal's logic level on the channel n of pin interrupt. Software cannot control it.

C2L – Capture 2 Low Byte

7	6	5	4	3	2	1	0
C2L[7:0]							
R/W							

Address: EDH Reset value: 0000 0000b

Bit	Name	Description
7:0	C2L[7:0]	**Input capture 2 result low byte** The C2L register is the low byte of the 16-bit result captured by input capture 2.

C2H – Capture 2 High Byte

7	6	5	4	3	2	1	0
C2H[7:0]							
R/W							

Address: EEH Reset value: 0000 0000b

Bit	Name	Description
7:0	C2H[7:0]	**Input capture 2 result high byte** The C2H register is the high byte of the 16-bit result captured by input capture 2.

EIP – Extensive Interrupt Priority[3]

7	6	5	4	3	2	1	0
PT2	PSPI	PFB	PWDT	PPWM	PCAP	PPI	PI2C
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: EFH Reset value: 0000 0000b

Bit	Name	Description
7	PT2	**Timer 2 interrupt priority low bit**
6	PSPI	**SPI interrupt priority low bit**
5	PFB	**Fault Brake interrupt priority low bit**
4	PWDT	**WDT interrupt priority low bit**
3	PPWM	**PWM interrupt priority low bit**
2	PCAP	**Input capture interrupt priority low bit**
1	PPI	**Pin interrupt priority low bit**
0	PI2C	**I^2C interrupt priority low bit**

[3] EIP is used in combination with the EIPH to determine the priority of each interrupt source. See Table 20-2. Interrupt Priority Level Setting for correct interrupt priority configuration.

B – B Register (Bit-addressable)

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F0H Reset value: 0000 0000b

Bit	Name	Description
7:0	B[7:0]	**B register** The B register is the other accumulator of the standard 80C51 .It is used mainly for MUL and DIV instructions.

CAPCON3 – Input Capture Control 3

7	6	5	4	3	2	1	0
CAP13	CAP12	CAP11	CAP10	CAP03	CAP02	CAP01	CAP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F1H Reset value: 0000 0000b

Bit	Name	Description
[7:4]	CAP1[3:0]	**Input capture channel 0 input pin select** 0000 = P1.2/IC0 0001 = P1.1/IC1 0010 = P1.0/IC2 0011 = P0.0/IC3 0100 = P0.4/IC3 0101 = P0.1/IC4 0110 = P0.3/IC5 0111 = P0.5/IC6 1000 = P1.5/IC7 others = P1.2/IC0

Bit	Name	Description
[3:0]	CAP0[3:0]	**Input capture channel 0 input pin select** 0000 = P1.2/IC0 0001 = P1.1/IC1 0010 = P1.0/IC2 0011 = P0.0/IC3 0100 = P0.4/IC3 0101 = P0.1/IC4 0110 = P0.3/IC5 0111 = P0.5/IC6 1000 = P1.5/IC7 others = P1.2/IC0

CAPCON4 – Input Capture Control 4

7	6	5	4	3	2	1	0
-	-	-	-	CAP23	CAP22	CAP21	CAP20
-	-	-	-	R/W	R/W	R/W	R/W

Address: F2H Reset value: 0000 0000b

Bit	Name	Description
[3:0]	CAP2[3:0]	**Input capture channel 0 input pin select** 0000 = P1.2/IC0 0001 = P1.1/IC1 0010 = P1.0/IC2 0011 = P0.0/IC3 0100 = P0.4/IC3 0101 = P0.1/IC4 0110 = P0.3/IC5 0111 = P0.5/IC6 1000 = P1.5/IC7 others = P1.2/IC0

SPCR – Serial Peripheral Control Register

7	6	5	4	3	2	1	0
SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F3H, page 0 Reset value: 0000 0000b

Bit	Name	Description
7	SSOE	**Slave select output enable** This bit is used in combination with the DISMODF (SPSR.3) bit to determine the feature of $\overline{SS}$ pin as shown in Table 14-1. Slave Select Pin Configurations. This bit takes effect only under MSTR = 1 and DISMODF = 1 condition. 0 = $\overline{SS}$ functions as a general purpose I/O pin. 1 = $\overline{SS}$ automatically goes low for each transmission when selecting external Slave device and goes high during each idle state to de-select the Slave device.
6	SPIEN	**SPI enable** 0 = SPI function Disabled. 1 = SPI function Enabled.

Bit	Name	Description
5	LSBFE	**LSB first enable** 0 = The SPI data is transferred MSB first. 1 = The SPI data is transferred LSB first.
4	MSTR	**Master mode enable** This bit switches the SPI operating between Master and Slave modes. 0 = The SPI is configured as Slave mode. 1 = The SPI is configured as Master mode.
3	CPOL	**SPI clock polarity select** CPOL bit determines the idle state level of the SPI clock. See Figure 14-4. SPI Clock Formats. 0 = The SPI clock is low in idle state. 1 = The SPI clock is high in idle state.
2	CPHA	**SPI clock phase select** CPHA bit determines the data sampling edge of the SPI clock. See Figure 14-4. SPI Clock Formats. 0 = The data is sampled on the first edge of the SPI clock. 1 = The data is sampled on the second edge of the SPI clock.

SPCR2 – Serial Peripheral Control Register 2

7	6	5	4	3	2	1	0
-	-	-	-	-	-	SPIS1	SPIS0
-	-	-	-	-	-	R/W	R/W

Address: F3H, page 1 Reset value: 0000 0000b

Bit	Name	Description
7:2	-	**Reserved**

Bit	Name	Description
1:0	SPIS[1:0]	**SPI Interval time selection between adjacent bytes** SPIS[1:0] and CPHA select eight grades of SPI interval time selection between adjacent bytes. As below table: CPHA SPIS1 SPIS0 SPI clock 0 0 0 0.5 0 0 1 1.0 0 1 0 1.5 0 1 1 2.0 1 0 0 1.0 1 0 1 1.5 1 1 0 2.0 1 1 1 2.5 SPIS[1:0] are valid only under Master mode (MSTR = 1).

SPSR – Serial Peripheral Status Register

7	6	5	4	3	2	1	0
SPIF	WCOL	SPIOVF	MODF	DISMODF	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-

Address: F4H Reset value: 0000 0000b

Bit	Name	Description
7	SPIF	**SPI complete flag** This bit is set to logic 1 via hardware while an SPI data transfer is complete or an receiving data has been moved into the SPI read buffer. If ESPI (EIE .0) and EA are enabled, an SPI interrupt will be required. This bit should be cleared via software. Attempting to write to SPDR is inhibited if SPIF is set.
6	WCOL	**Write collision error flag** This bit indicates a write collision event. Once a write collision event occurs, this bit will be set. It should be cleared via software.
5	SPIOVF	**SPI overrun error flag** This bit indicates an overrun event. Once an overrun event occurs, this bit will be set. If ESPI and EA are enabled, an SPI interrupt will be required. This bit should be cleared via software.
4	MODF	**Mode Fault error flag** This bit indicates a Mode Fault error event. If $\overline{SS}$ pin is configured as Mode Fault input (MSTR = 1 and DISMODF = 0) and $\overline{SS}$ is pulled low by external devices, a Mode Fault error occurs. Instantly MODF will be set as logic 1. If ESPI and EA are enabled, an SPI interrupt will be required. This bit should be cleared via software.
3	DISMODF	**Disable Mode Fault error detection** This bit is used in combination with the SSOE (SPCR.7) bit to determine the feature of $\overline{SS}$ pin as shown in Table 14-1. Slave Select Pin Configurations. DISMODF is valid only in Master mode (MSTR = 1). 0 = Mode Fault detection Enabled. $\overline{SS}$ serves as input pin for Mode Fault detection disregard of SSOE. 1 = Mode Fault detection Disabled. The feature of $\overline{SS}$ follows SSOE bit.

SPDR – Serial Peripheral Data Register

7	6	5	4	3	2	1	0
SPDR[7:0]							
R/W							

Address: F5H Reset value: 0000 0000b

Bit	Name	Description
7:0	SPDR[7:0]	**Serial peripheral data** This byte is used for transmitting or receiving data on SPI bus. A write of this byte is a write to the shift register. A read of this byte is actually a read of the read data buffer. In Master mode, a write to this register initiates transmission and reception of a byte simultaneously.

AINDIDS – ADC Channel Digital Input Disconnect

7	6	5	4	3	2	1	0
P11DIDS	P03DIDS	P04DIDS	P05DIDS	P06DIDS	P07DIDS	P30DIDS	P17DIDS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F6H Reset value: 0000 0000b

Bit	Name	Description
n	PnnDIDS	**ADC Channel digital input disable** 0 = ADC channel n digital input Enabled. 1 = ADC channel n digital input Disabled. ADC channel n is read always 0.

EIPH – Extensive Interrupt Priority High[4]

7	6	5	4	3	2	1	0
PT2H	PSPIH	PFBH	PWDTH	PPWMH	PCAPH	PPIH	PI2CH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F7H Reset value: 0000 0000b

Bit	Name	Description
7	PT2H	**Timer 2 interrupt priority high bit**
6	PSPIH	**SPI interrupt priority high bit**
5	PFBH	**Fault Brake interrupt priority high bit**
4	PWDTH	**WDT interrupt priority high bit**
3	PPWMH	**PWM interrupt priority high bit**
2	PCAPH	**Input capture interrupt priority high bit**
1	PPIH	**Pin interrupt priority high bit**
0	PI2CH	**I^2C interrupt priority high bit**

[4] EIPH is used in combination with the EIP to determine the priority of each interrupt source. See Table 20-2. Interrupt Priority Level Setting for correct interrupt priority configuration.

SCON_1 – Serial Port 1 Control (bit-addressable)

7	6	5	4	3	2	1	0
SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F8H Reset value: 0000 0000b

Bit	Name	Description
7	SM0_1/FE_1	**Serial port 1 mode select** SMOD0_1 (T3CON.6) = 0: See Table 13-2. Serial Port 1 Mode Description for details. SMOD0_1 (T3CON.6) = 1: SM0_1/FE_1 bit is used as frame error (FE) status flag. It is cleared by software. 0 = Frame error (FE) did not occur. 1 = Frame error (FE) occurred and detected.
6	SM1_1	
5	SM2_1	**Multiprocessor communication mode enable** The function of this bit is dependent on the serial port 1 mode. Mode 0: No effect. Mode 1: This bit checks valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is valid only when the received stop bit is logic 1 and the received data matches “Given” or “Broadcast” address. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is valid only when the received 9th bit is logic 1 and the received data matches “Given” or “Broadcast” address.
4	REN_1	**Receiving enable** 0 = Serial port 1 reception Disabled. 1 = Serial port 1 reception Enabled in Mode 1,2, or 3. In Mode 0, reception is initiated by the condition REN_1 = 1 and RI_1 = 0.
3	TB8_1	**9th transmitted bit** This bit defines the state of the 9th transmission bit in serial port 1 Mode 2 or 3. It is not used in Mode 0 or 1.
2	RB8_1	**9th received bit** The bit identifies the logic level of the 9th received bit in serial port 1 Mode 2 or 3. In Mode 1, RB8_1 is the logic level of the received stop bit. SM2_1 bit as logic 1 has restriction for exception. RB8_1 is not used in Mode 0.
1	TI_1	**Transmission interrupt flag** This flag is set by hardware when a data frame has been transmitted by the serial port 1 after the 8th bit in Mode 0 or the last data bit in other modes. When the serial port 1 interrupt is enabled, setting this bit causes the CPU to execute the serial port 1 interrupt service routine. This bit must be cleared manually via software.

Bit	Name	Description
0	RI_1	**Receiving interrupt flag** This flag is set via hardware when a data frame has been received by the serial port 1 after the 8th bit in Mode 0 or after sampling the stop bit in Mode 1, 2, or 3. SM2_1 bit as logic 1 has restriction for exception. When the serial port 1 interrupt is enabled, setting this bit causes the CPU to execute to the serial port 1 interrupt service routine. This bit must be cleared manually via software.

PDTEN – PWM Dead-time Enable (TA protected)

7	6	5	4	3	2	1	0
-	-	-	PDTCNT.8	-	PDT45EN	PDT23EN	PDT01EN
-	-	-	R/W	-	R/W	R/W	R/W

Address: F9H Reset value: 0000 0000b

Bit	Name	Description
4	PDTCNT.8	**PWM dead-time counter bit 8** See PDTCNT register.
2	PDT45EN	**PWM4/5 pair dead-time insertion enable** This bit is valid only when PWM4/5 is under complementary mode. 0 = No delay on GP4/GP5 pair signals. 1 = Insert dead-time delay on the rising edge of GP4/GP5 pair signals.
1	PDT23EN	**PWM2/3 pair dead-time insertion enable** This bit is valid only when PWM2/3 is under complementary mode. 0 = No delay on GP2/GP3 pair signals. 1 = Insert dead-time delay on the rising edge of GP2/GP3 pair signals.
0	PDT01EN	**PWM0/1 pair dead-time insertion enable** This bit is valid only when PWM0/1 is under complementary mode. 0 = No delay on GP0/GP1 pair signals. 1 = Insert dead-time delay on the rising edge of GP0/GP1 pair signals.

PDTCNT – PWM Dead-time Counter (TA protected)

7	6	5	4	3	2	1	0
PDTCNT[7:0]							
R/W							

Address: FAH Reset value: 0000 0000b

Bit	Name	Description
7:0	PDTCNT[7:0]	**PWM dead-time counter low byte** This 8-bit field combined with PDTEN.4 forms a 9-bit PWM dead-time counter PDTCNT. This counter is valid only when PWM is under complementary mode and the correspond PDTEN bit for PWM pair is set. PWM dead-time = $\frac{PDTCNT+1}{F_{SYS}}$. Note that user should not modify PDTCNT during PWM run time.

PMEN – PWM Mask Enable

7	6	5	4	3	2	1	0
-	-	PMEN5	PMEN4	PMEN3	PMEN2	PMEN1	PMEN0
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Address: FBH Reset value: 0000 0000b

Bit	Name	Description
n	PMENn	**PWMn mask enable** 0 = PWMn signal outputs from its PWM generator. 1 = PWMn signal is masked by PMDn.

PMD – PWM Mask Data

7	6	5	4	3	2	1	0
-	-	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Address: FCH Reset value: 0000 0000b

Bit	Name	Description
n	PMDn	**PWMn mask data** The PWMn signal outputs mask data once its corresponding PMENn is set. 0 = PWMn signal is masked by 0. 1 = PWMn signal is masked by 1.

PORDIS – POR disable (TA protected)

7	6	5	4	3	2	1	0
PORDIS[7:0]							
W							

Address: FDH, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
7:0	PORDIS[7:0]	**POR disable** To first writing 5AH to the PORDIS and immediately followed by a writing of A5H will disable POR.

Notice: Strongly suggests that disable POR function after power-on reset at the initial part of Customer code. Please reference 24.1 Power-On Reset (POR) for more detail information.

EIP1 – Extensive Interrupt Priority 1[5]

7	6	5	4	3	2	1	0
-	-	-	-	-	PWKT	PT3	PS_1
-	-	-	-	-	R/W	R/W	R/W

Address: FEH, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
2	PWKT	**WKT interrupt priority low bit**
1	PT3	**Timer 3 interrupt priority low bit**
0	PS_1	**Serial port 1 interrupt priority low bit**

[5] EIP1 is used in combination with the EIPH1 to determine the priority of each interrupt source. See Table 20-2. Interrupt Priority Level Setting for correct interrupt priority configuration.

EIPH1 – Extensive Interrupt Priority High 1[6]

7	6	5	4	3	2	1	0
-	-	-	-	-	PWKTH	PT3H	PSH_1
-	-	-	-	-	R/W	R/W	R/W

Address: FFH, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
2	PWKTH	**WKT interrupt priority high bit**
1	PT3H	**Timer 3 interrupt priority high bit**
0	PSH_1	**Serial port 1 interrupt priority high bit**

[6] EIPH1 is used in combination with the EIP1 to determine the priority of each interrupt source. See Table 20-2. Interrupt Priority Level Setting for correct interrupt priority configuration.

7. I/O PORT STRUCTURE AND OPERATION

The N76E003 has a maximum of 26 bit-addressable general I/O pins grouped as 4 ports, P0 to P3. Each port has its port control register (Px register). The writing and reading of a port control register have different meanings. A write to port control register sets the port output latch logic value, whereas a read gets the port pin logic state. All I/O pins except P2.0 can be configured individually as one of four I/O modes by software. These four modes are quasi-bidirectional (standard 8051 port structure), push-pull, input-only, and open-drain modes. Each port spends two special function registers PxM1 and PxM2 to select the I/O mode of port Px. The list below illustrates how to select the I/O mode of Px.n. Note that the default configuration of is input-only (high-impedance) after any reset.

Table 7-1. Configuration for Different I/O Modes

PxM1.n	PxM2.n	I/O Type
0	0	Quasi-bidirectional
0	1	Push-pull
1	0	Input-only (high-impedance)
1	1	Open-drain

All I/O pins can be selected as TTL level inputs or Schmitt triggered inputs by selecting corresponding bit in PxS register. Schmitt triggered input has better glitch suppression capability. All I/O pins also have bit-controllable, slew rate select ability via software. The control registers are PxSR. By default, the slew rate is slow. If user would like to increase the I/O output speed, setting the corresponding bit in PxSR, the slew rate is selected in a faster level.

P2.0 is configured as an input-only pin when programming RPD (CONFIG0.2) as 0. Meanwhile, P2.0 is permanent in input-only mode and Schmitt triggered type. P2.0 also has an internal pull-up enabled by P20UP (P2S.7). If RPD remains un-programmed, P2.0 pin functions as an external reset pin and P2.0 is not available. A read of P2.0 bit is always 0. Meanwhile, the internal pull-up is always enabled.

7.1 Quasi-Bidirectional Mode

The quasi-bidirectional mode, as the standard 8051 I/O structure, can rule as both input and output. When the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a large current. In the quasi-bidirectional I/O structure, there are three pull-high transistors. Each of them serves different purposes. One of these pull-highs, called the “very weak” pull-high, is turned on whenever the port latch contains logic 1. he “very weak” pull-high sources a very small current that will pull the pin high if it is left floating.

A second pull-high, called the “weak” pull-high, is turned on when the outside port pin itself is at logic 1 level. This pull-high provides the primary source current for a quasi-bidirectional pin that is outputting 1. If a pin which has logic 1 on it is pulled low by an external device, the “weak” pull-high turns off, and only the “very weak” pull-high remains on. To pull the pin low under these conditions, the external device has to sink enough current (larger than I_{TL}) to overcome the “weak” pull-high and make the voltage on the port pin below its input threshold (lower than V_{IL}).

The third pull-high is the “strong” pull-high. This pull-high is used to speed up 0-to-1 transitions on a quasi-bidirectional port pin when the port latch changes from logic 0 to logic 1. When this occurs, the strong pull-high turns on for two-CPU-clock time to pull the port pin high quickly. Then it turns off and “weak” and “very weak” pull-highs continue remaining the port pin high. The quasi-bidirectional port structure is shown below.

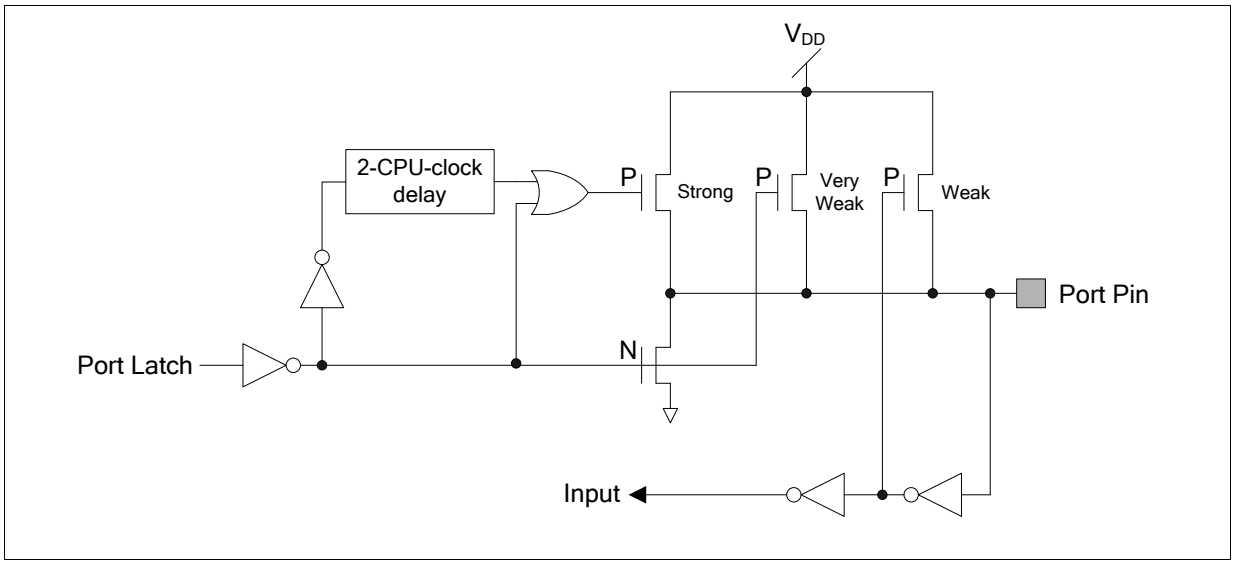


Figure 7-1. Quasi-Bidirectional Mode Structure

7.2 Push-Pull Mode

The push-pull mode has the same pull-low structure as the quasi-bidirectional mode, but provides a continuous strong pull-high when the port latch is written by logic 1. The push-pull mode is generally used as output pin when more source current is needed for an output driving.

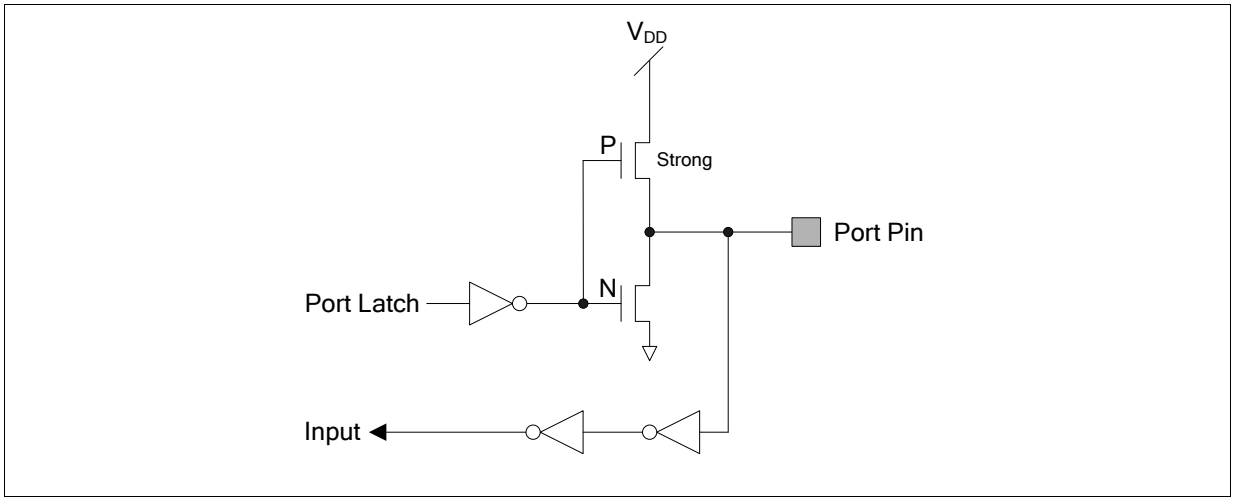


Figure 7-2. Push-Pull Mode Structure

7.3 Input-Only Mode

Input-only mode provides true high-impedance input path. Although a quasi-bidirectional mode I/O can also be an input pin, but it requires relative strong input source. Input-only mode also benefits to power consumption reduction for logic 0 input always consumes current from V_{DD} if in quasi-bidirectional mode. User needs to take care that an input-only mode pin should be given with a determined voltage level by external devices or resistors. A floating pin will induce leakage current especially in Power-down mode.

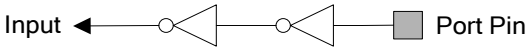


Figure 7-3. Input-Only Mode Structure

7.4 Open-Drain Mode

The open-drain mode turns off all pull-high transistors and only drives the pull-low of the port pin when the port latch is given by logic 0. If the port latch is logic 1, it behaves as if in input-only mode. To be used as an output pin generally as I^2C lines, an open-drain pin should add an external pull-high, typically a resistor tied to V_{DD}. User needs to take care that an open-drain pin with its port latch as logic 1 should be given with a determined voltage level by external devices or resistors. A floating pin will induce leakage current especially in Power-down mode.

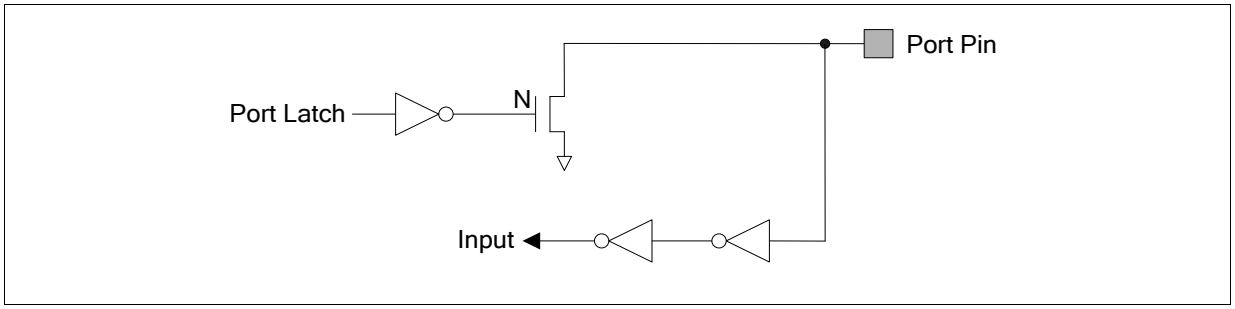


Figure 7-4. Open-Drain Mode Structure

7.5 Read-Modify-Write Instructions

nstructions that read a byte from F or internal A , modify it, and rewrite it back, are called " e ad-Modify-Write" instructions. When the destination is an O port or a port bit, these instructions read the internal output latch rather than the external pin state. This kind of instructions read the port SFR value, modify it and write back to the port SFR. All "Read-Modify-Write" instructions are listed as follows.

Instruction		Description
ANL		Logical AND. (ANL direct, A and ANL direct, #data)
ORL		Logical OR. (ORL direct, A and ORL direct, #data)
XRL		Logical exclusive OR. (XRL direct, A and XRL direct, #data)
JBC		Jump if bit = 1 and clear it. (JBC bit, rel)
CPL		Complement bit. (CPL bit)
INC		Increment. (INC direct)
DEC		Decrement. (DEC direct)
DJNZ		Decrement and jump if not zero. (DJNZ direct, rel)
MOV	bit, C	Move carry to bit. (MOV bit, C)
CLR	bit	Clear bit. (CLR bit)
SETB	bit	Set bit. (SETB bit)

The last three seem not obviously " ea d-Modify-Write" instructions but actually they are. They read the entire port latch value, modify the changed bit, and then write the new value back to the port latch.

7.6 Control Registers of I/O Ports

The N76E003 has a lot of I/O control registers to provide flexibility in all kinds of applications. The SFRs related with I/O ports can be categorized into four groups: input and output control, output mode control, input type and sink current control, and output slew rate control. All of SFRs are listed as follows.

7.6.1 Input and Output Data Control

These registers are I/O input and output data buffers. Reading gets the I/O input data. Writing forces the data output. All of these registers are bit-addressable.

P0 – Port 0 (Bit-addressable)

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 80H Reset value: 1111 1111b

Bit	Name	Description
7:0	P0[7:0]	**Port 0** Port 0 is an maximum 8-bit general purpose I/O port.

P1 – Port 1 (Bit-addressable)

7	6	5	4	3	2	1	0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 90H Reset value: 1111 1111b

Bit	Name	Description
7:0	P1[7:0]	**Port 1** Port 1 is an maximum 8-bit general purpose I/O port.

P2 – Port 2 (Bit-addressable)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	P2.0
R	R	R	R	R	R	R	R

Address: A0H Reset value: 0000 000Xb

Bit	Name	Description
7:1	0	**Reserved** The bits are always read as 0.
0	P2.0	**Port 2 bit 0** P2.0 is an input-only pin when RPD (CONFIG0.2) is programmed as 0. When leaving RPD un-programmed, P2.0 is always read as 0.

P3 – Port 3 (Bit-addressable)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	P3.0
R	R	R	R	R	R	R	R/W

Address: B0H Reset value: 0000 0001b

Bit	Name	Description
7:1	0	**Reserved** The bits are always read as 0.
0	P3.0	**Port 3 bit 0** P3.0 is available only when the internal oscillator is used as the system clock. At this moment, P3.0 functions as a general purpose I/O. If the system clock is not selected as the internal oscillator, P3.0 pin functions as OSCIN. A write to P3.0 is invalid and P3.0 is always read as 0.

7.6.2 Output Mode Control

These registers control output mode which is configurable among four modes: input-only, quasi-bidirectional, push-pull, or open-drain. Each pin can be configured individually. There is also a pull-up control for P2.0 in P2S.7.

P0M1 – Port 0 Mode Select 1[1]

7	6	5	4	3	2	1	0
P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B1H, Page: 0 Reset value: 1111 1111b

Bit	Name	Description
7:0	P0M1[7:0]	**Port 0 mode select 1**

P0M2 – Port 0 Mode Select 2[1]

7	6	5	4	3	2	1	0
P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B2H, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
7:0	P0M2[7:0]	**Port 0 mode select 2**

[1] P0M1 and P0M2 are used in combination to determine the I/O mode of each pin of P0. See Table 7-1. Configuration for Different I/O Modes.

P1M1 – Port 1 Mode Select 1[2]

7	6	5	4	3	2	1	0
P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B3H, Page: 0 Reset value: 1111 1111b

Bit	Name	Description
7:0	P1M1[7:0]	**Port 1 mode select 1**

P1M2 – Port 1 Mode Select 2[2]

7	6	5	4	3	2	1	0
P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B4H, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
7:0	P1M2[7:0]	**Port 1 mode select 2.**

[2] P1M1 and P1M2 are used in combination to determine the I/O mode of each pin of P1. See Table 7-1. Configuration for Different I/O Modes.

P1M1.n	P1M2.n	I/O Type
0	0	Quasi-bidirectional
0	1	Push-pull
1	0	Input-only (high-impedance)
1	1	Open-drain

P2S – P20 Setting and Timer01 Output Enable

7	6	5	4	3	2	1	0
P20UP	-	-	-	T1OE	T0OE	-	P2S.0
R/W	-	-	-	R/W	R/W	-	R/W

Address: B5H Reset value: 0000 0000b

Bit	Name	Description
7	P20UP	**P2.0 pull-up enable** 0 = P2.0 pull-up Disabled. 1 = P2.0 pull-up Enabled. This bit is valid only when RPD (CONFIG0.2) is programmed as 0. When selecting as a $\overline{\text{RST}}$ pin, the pull-up is always enabled.

P3M1 – Port 3 Mode Select 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3M1.0[3]
-	-	-	-	-	-	-	R/W

Address: ACH, Page: 0 Reset value: 0000 0001b

Bit	Name	Description
0	P3M1.0	**Port 3 mode select 1**

P3M2 – Port 3 Mode Select 2

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3M2.0[3]
-	-	-	-	-	-	-	R/W

Address: ADH, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
0	P3M2.0	**Port 3 mode select 2**

[3] P3M1 and P3M2 are used in combination to determine the I/O mode of each pin of P3. See Table 7-1. Configuration for Different I/O Modes.

P3M1.n	P3M2.n	I/O Type
0	0	Quasi-bidirectional
0	1	Push-pull
1	0	Input-only (high-impedance)
1	1	Open-drain

7.6.3 Input Type

Each I/O pin can be configured individually as TTL input or Schmitt triggered input. Note that all of PxS registers are accessible by switching SFR page to page 1.

P0S – Port 0 Schmitt Triggered Input

7	6	5	4	3	2	1	0
P0S.7	P0S.6	P0S.5	P0S.4	P0S.3	P0S.2	P0S.1	P0S.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B1H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
n	P0S.n	**P0.n Schmitt triggered input** 0 = TTL level input of P0.n. 1 = Schmitt triggered input of P0.n.

P1S – Port 1 Schmitt Triggered Input

7	6	5	4	3	2	1	0
P1S.7	P1S.6	P1S.5	P1S.4	P1S.3	P1S.2	P1S.1	P1S.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B3H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
7	P1S.7	**P1.7 Schmitt triggered input** 0 = TTL level input of P1.7. 1 = Schmitt triggered input of P1.7.
6	P1S.6	**P1.6 Schmitt triggered input** 0 = TTL level input of P1.6. 1 = Schmitt triggered input of P1.6.
5	P1S.5	**P1.5 Schmitt triggered input** 0 = TTL level input of P1.5. 1 = Schmitt triggered input of P1.5.
4	P1S.4	**P1.4 Schmitt triggered input** 0 = TTL level input of P1.4. 1 = Schmitt triggered input of P1.4.
3	P1S.3	**P1.3 Schmitt triggered input** 0 = TTL level input of P1.3. 1 = Schmitt triggered input of P1.3.
2	P1S.2	**P1.2 Schmitt triggered input** 0 = TTL level input of P1.2. 1 = Schmitt triggered input of P1.2.
1	P1S.1	**P1.1 Schmitt triggered input** 0 = TTL level input of P1.1. 1 = Schmitt triggered input of P1.1.
0	P1S.0	**P1.0 Schmitt triggered input** 0 = TTL level input of P1.0. 1 = Schmitt triggered input of P1.0.

P2S – P20 Setting and Timer01 Output Enable

7	6	5	4	3	2	1	0
P20UP	-	-	-	T1OE	T0OE	-	P2S.0
R/W	-	-	-	R/W	R/W	-	R/W

Address: B5H Reset value: 0000 0000b

Bit	Name	Description
0	P2S.0	**P2.0 Schmitt triggered input** 0 = TTL level input of P2.0. 1 = Schmitt triggered input of P2.0.

P3S – Port 3 Schmitt Triggered Input

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3S.0
-	-	-	-	-	-	-	R/W

Address: ACH, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
0	P3S.0	**P3.0 Schmitt triggered input** 0 = TTL level input of P3.0. 1 = Schmitt triggered input of P3.0.

7.6.4 Output Slew Rate Control

Slew rate for each I/O pin is configurable individually. By default, each pin is in normal slew rate mode. User can set each control register bit to enable high-speed slew rate for the corresponding I/O pin. Note that all PxSR registers are accessible by switching SFR page to page 1.

P0SR – Port 0 Slew Rate

7	6	5	4	3	2	1	0
P0SR.7	P0SR.6	P0SR.5	P0SR.4	P0SR.3	P0SR.2	P0SR.1	P0SR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B2H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
n	P0SR.n	**P0.n slew rate** 0 = P0.n normal output slew rate. 1 = P0.n high-speed output slew rate.

P1SR – Port 1 Slew Rate

7	6	5	4	3	2	1	0
P1SR.7	P1SR.6	P1SR.5	P1SR.4	P1SR.3	P1SR.2	P1SR.1	P1SR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B4H, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
n	P1SR.n	**P1.n slew rate** 0 = P1.n normal output slew rate. 1 = P1.n high-speed output slew rate.

P3SR – Port 3 Slew Rate

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P3SR.0
-	-	-	-	-	-	-	R/W

Address: ADH, Page: 1 Reset value: 0000 0000b

Bit	Name	Description
0	P3SR.0	**P3.n slew rate** 0 = P3.0 normal output slew rate. 1 = P3.0 high-speed output slew rate.

8. TIMER/COUNTER 0 AND 1

Timer/Counter 0 and 1 on N76E003 are two 16-bit Timers/Counters. Each of them has two 8-bit registers those form the 16-bit counting register. For Timer/Counter 0 they are TH0, the upper 8-bit register, and TL0, the lower 8-bit register. Similarly Timer/Counter 1 has two 8-bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

The Timer or Counter function is selected by the $\overline{\quad}$ bit in TMOD. Each Timer/Counter has its own selection bit. TMOD.2 selects the function for Timer/Counter 0 and TMOD.6 selects the function for Timer/Counter 1

When configured as a “Timer”, the timer counts the system clock cycles. The timer clock is 1/12 of the system clock (F_{SYS}) for standard 8051 capability or direct the system clock for enhancement, which is selected by T0M (CKCON.3) bit for Timer 0 and T1M (CKCON.4) bit for Timer 1. In the “Counter” mode, the countering register increases on the falling edge of the external input pin T0. If the sampled value is high in one clock cycle and low in the next, a valid 1-to-0 transition is recognized on T0 or T1 pin.

The Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits T0OE and T1OE in the P2S register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be logic 1 prior to the first timer overflow when this mode is turned on. In order for this mode to function, the $\overline{\quad}$ bit should be cleared selecting the system clock as the clock source for the timer.

Note that the TH0 (TH1) and TL0 (TL1) are accessed separately. It is strongly recommended that in mode 0 or 1, user should stop Timer temporally by clearing TR0 (TR1) bit before reading from or writing to TH0 (TH1) and TL0 (TL1). The free-running reading or writing may cause unpredictable result.

TMOD – Timer 0 and 1 Mode

7	6	5	4	3	2	1	0
GATE	$\overline{\quad}$	M1	M0	GATE	$\overline{\quad}$	M1	M0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 89H Reset value: 0000 0000b

Bit	Name	Description
7	GATE	**Timer 1 gate control** 0 = Timer 1 will clock when TR1 is 1 regardless of $\overline{\quad\quad}$ logic level. 1 = Timer 1 will clock only when TR1 is 1 and $\overline{\quad\quad}$ is logic 1.

Bit	Name	Description
6	$\overline{T1}$	**Timer 1 Counter/Timer select** 0 = Timer 1 is incremented by internal system clock. 1 = Timer 1 is incremented by the falling edge of the external pin T1.
5	M1	**Timer 1 mode select** M1 M0 Timer 1 Mode 0 0 Mode 0: 13-bit Timer/Counter 0 1 Mode 1: 16-bit Timer/Counter 1 0 Mode 2: 8-bit Timer/Counter with auto-reload from TH1 1 1 Mode 3: Timer 1 halted
4	M0	
3	GATE	**Timer 0 gate control** 0 = Timer 0 will clock when TR0 is 1 regardless of $\overline{INT0}$ logic level. 1 = Timer 0 will clock only when TR0 is 1 and $\overline{INT0}$ is logic 1.
2	$\overline{T0}$	**Timer 0 Counter/Timer select** 0 = Timer 0 is incremented by internal system clock. 1 = Timer 0 is incremented by the falling edge of the external pin T0.
1	M1	**Timer 0 mode select** M1 M0 Timer 0 Mode 0 0 Mode 0: 13-bit Timer/Counter 0 1 Mode 1: 16-bit Timer/Counter 1 0 Mode 2: 8-bit Timer/Counter with auto-reload from TH0 1 1 Mode 3: TL0 as a 8-bit Timer/Counter and TH0 as a 8-bit Timer
0	M0	

TCON – Timer 0 and 1 Control (Bit-addressable)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R (level) R/W (edge)	R/W	R (level) R/W (edge)	R/W

Address: 88H Reset value: 0000 0000b

Bit	Name	Description
7	TF1	**Timer 1 overflow flag** This bit is set when Timer 1 overflows. It is automatically cleared by hardware when the program executes the Timer 1 interrupt service routine. This bit can be set or cleared by software.
6	TR1	**Timer 1 run control** 0 = Timer 1 Disabled. Clearing this bit will halt Timer 1 and the current count will be preserved in TH1 and TL1. 1 = Timer 1 Enabled.
5	TF0	**Timer 0 overflow flag** This bit is set when Timer 0 overflows. It is automatically cleared via hardware when the program executes the Timer 0 interrupt service routine. This bit can be set or cleared by software.
4	TR0	**Timer 0 run control** 0 = Timer 0 Disabled. Clearing this bit will halt Timer 0 and the current count will be preserved in TH0 and TL0. 1 = Timer 0 Enabled.

TL0 – Timer 0 Low Byte

7	6	5	4	3	2	1	0
TL0[7:0]							
R/W							

Address: 8AH Reset value: 0000 0000b

Bit	Name	Description
7:0	TL0[7:0]	**Timer 0 low byte** The TL0 register is the low byte of the 16-bit counting register of Timer 0.

TH0 – Timer 0 High Byte

7	6	5	4	3	2	1	0
TH0[7:0]							
R/W							

Address: 8CH Reset value: 0000 0000b

Bit	Name	Description
7:0	TH0[7:0]	**Timer 0 high byte** The TH0 register is the high byte of the 16-bit counting register of Timer 0.

TL1 – Timer 1 Low Byte

7	6	5	4	3	2	1	0
TL1[7:0]							
R/W							

Address: 8BH Reset value: 0000 0000b

Bit	Name	Description
7:0	TL1[7:0]	**Timer 1 low byte** The TL1 register is the low byte of the 16-bit counting register of Timer 1.

TH1 – Timer 1 High Byte

7	6	5	4	3	2	1	0
TH1[7:0]							
R/W							

Address: 8DH Reset value: 0000 0000b

Bit	Name	Description
7:0	TH1[7:0]	**Timer 1 high byte** The TH1 register is the high byte of the 16-bit counting register of Timer 1.

CKCON – Clock Control

7	6	5	4	3	2	1	0
-	PWMCKS	-	T1M	T0M	-	CLOEN	-
-	R/W	-	R/W	R/W	-	R/W	-

Address: 8EH Reset value: 0000 0000b

Bit	Name	Description
4	T1M	**Timer 1 clock mode select** 0 = The clock source of Timer 1 is the system clock divided by 12. It maintains standard 8051 compatibility. 1 = The clock source of Timer 1 is direct the system clock.
3	T0M	**Timer 0 clock mode select** 0 = The clock source of Timer 0 is the system clock divided by 12. It maintains standard 8051 compatibility. 1 = The clock source of Timer 0 is direct the system clock.

P2S – P20 Setting and Timer01 Output Enable

7	6	5	4	3	2	1	0
P20UP	-	-	-	T1OE	T0OE	-	P2S.0
R/W	-	-	-	R/W	R/W	-	R/W

Address: B5H Reset value: 0000 0000b

Bit	Name	Description
3	T1OE	**Timer 1 output enable** 0 = Timer 1 output Disabled. 1 = Timer 1 output Enabled from T1 pin. ot e that imer output should be enabled only when operating in its " imer" mode.
2	T0OE	**Timer 0 output enable** 0 = Timer 0 output Disabled. 1 = Timer 0 output Enabled from T0 pin. ot e that imer output should be enabled only when operating in its " imer" mode.

8.1 Mode 0 (13-Bit Timer)

In Mode 0, the Timer/Counter is a 13-bit counter. The 13-bit counter consists of TH0 (TH1) and the five lower bits of TL0 (TL1). The upper three bits of TL0 (TL1) are ignored. The Timer/Counter is enabled when TR0 (TR1) is set and either GATE is 0 or ____ (____) is 1. Gate setting as 1 allows the Timer to calculate the pulse width on external input pin ____ (____). When the 13-bit value moves from 1FFFH to 0000H, the Timer overflow flag TF0 (TF1) is set and an interrupt occurs if enabled.

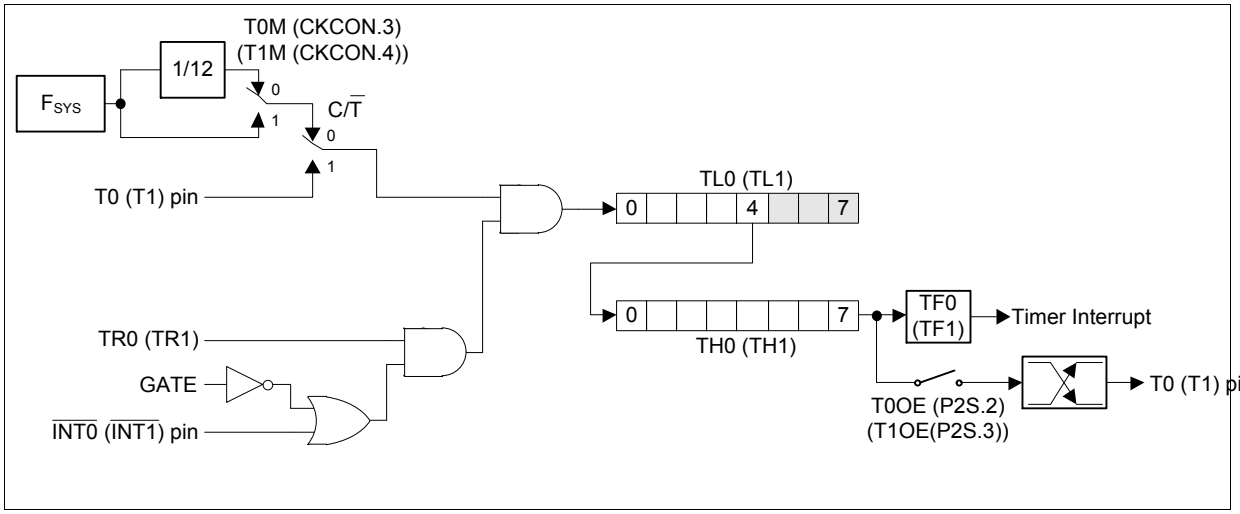


Figure 8-1. Timer/Counters 0 and 1 in Mode 0

8.2 Mode 1 (16-Bit Timer)

Mode 1 is similar to Mode 0 except that the counting registers are fully used as a 16-bit counter. Roll-over occurs when a count moves FFFFH to 0000H. The Timer overflow flag TF0 (TF1) of the relevant Timer/Counter is set and an interrupt will occurs if enabled.

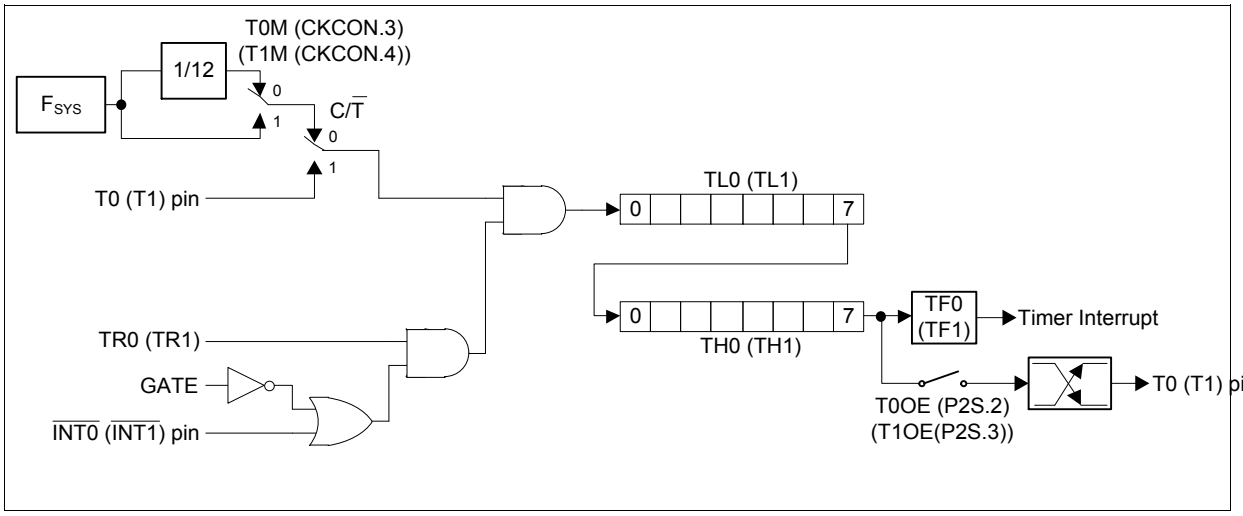


Figure 8-2. Timer/Counters 0 and 1 in Mode 1

8.3 Mode 2 (8-Bit Auto-Reload Timer)

In Mode 2, the Timer/Counter is in auto-reload mode. In this mode, TL0 (TL1) acts as an 8-bit count register whereas TH0 (TH1) holds the reload value. When the TL0 (TL1) register overflow, the TF0 (TF1) bit in TCON is set and TL0 (TL1) is reloaded with the contents of TH0 (TH1) and the counting process continues from here. The reload operation leaves the contents of the TH0 (TH1) register

unchanged. This feature is best suitable for UART baud rate generator for it runs without continuous software intervention. Note that only Timer1 can be the baud rate source for UART. Counting is enabled by setting the TR0 (TR1) bit as 1 and proper setting of GATE and ____ (____) pins. The functions of GATE and ____ (____) pins are just the same as Mode 0 and 1.

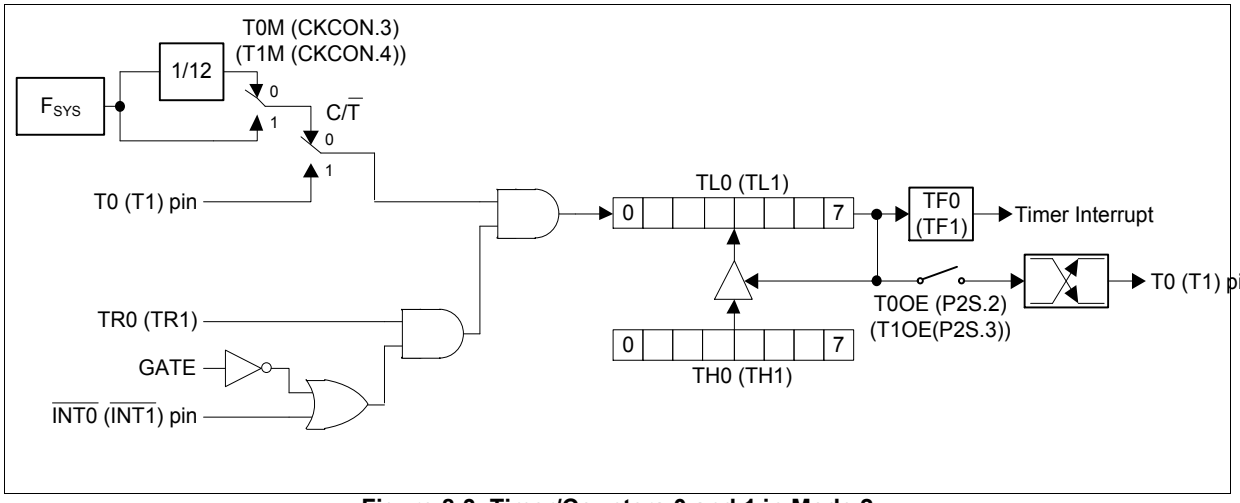


Figure 8-3. Timer/Counters 0 and 1 in Mode 2

8.4 Mode 3 (Two Separate 8-Bit Timers)

Mode 3 has different operating methods for Timer 0 and Timer 1. For Timer/Counter 1, Mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. TL0 uses the Timer/Counter 0 control bits ¯, GATE, TR0, ____, and TF0. The TL0 also can be used as a 1-to-0 transition counter on pin T0 as determined by ¯ (TMOD.2). TH0 is forced as a clock cycle counter and takes over the usage of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in case that an extra 8 bit timer is needed. If Timer/Counter 0 is configured in Mode 3, Timer/Counter 1 can be turned on or off by switching it out of or into its own Mode 3. It can still be used in Modes 0, 1 and 2 although its flexibility is restricted. It no longer has control over its overflow flag TF1 and the enable bit TR1. However Timer 1 can still be used as a Timer/Counter and retains the use of GATE, ____ pin and T1M. It can be used as a baud rate generator for the serial port or other application not requiring an interrupt.

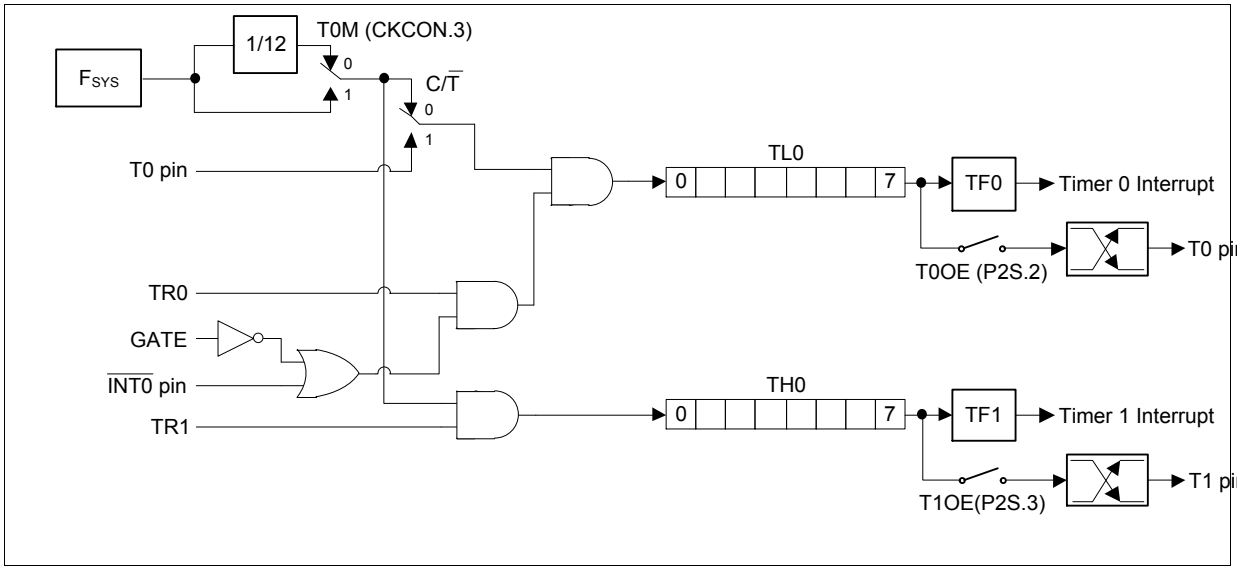
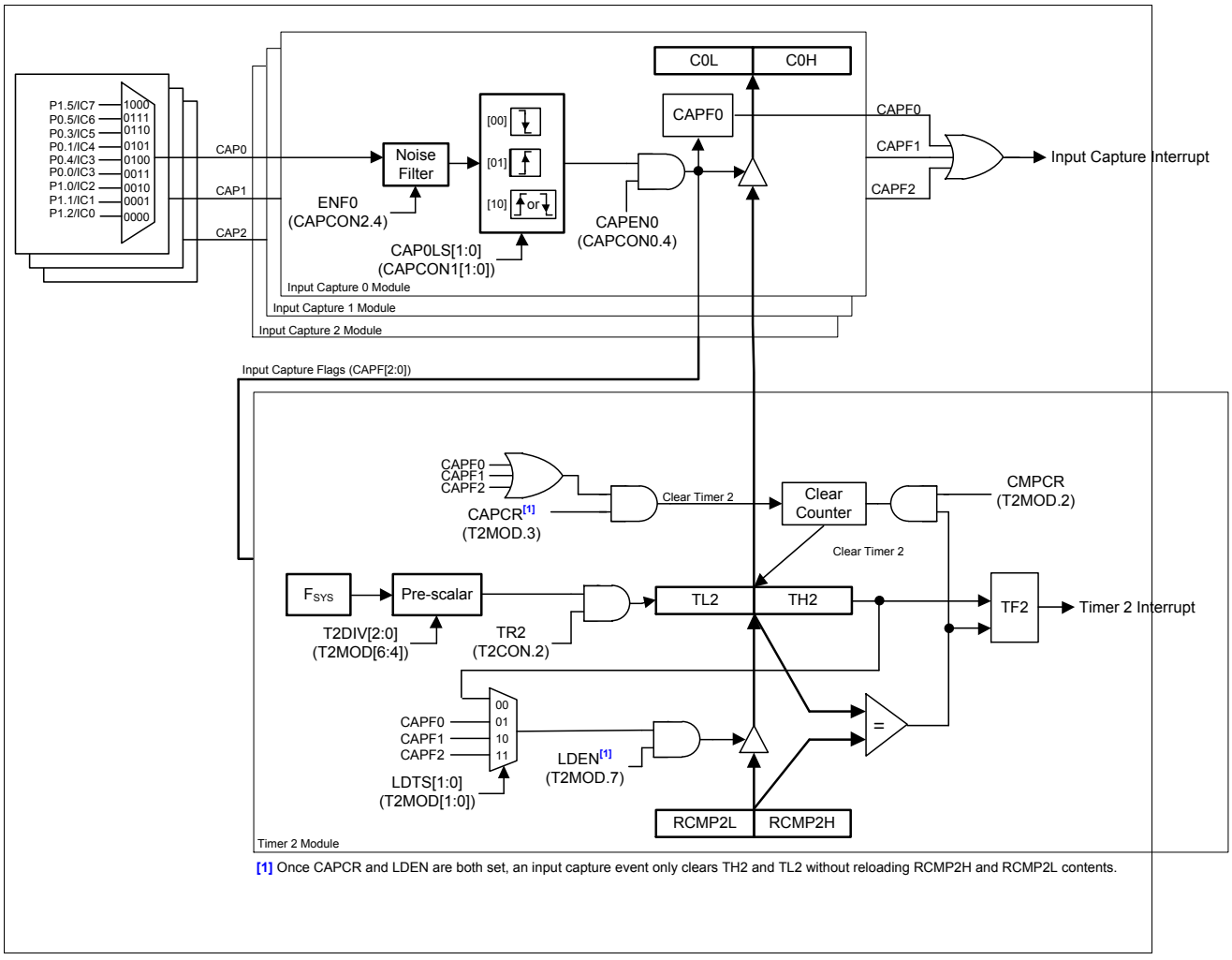


Figure 8-4. Timer/Counter 0 in Mode 3

9. TIMER 2 AND INPUT CAPTURE

Timer 2 is a 16-bit up counter cascaded with TH2, the upper 8 bits register, and TL2, the lower 8 bit register. Equipped with RCMP2H and RCMP2L, Timer 2 can operate under compare mode and auto-reload mode selected by $\overline{\text{T2CON.0}}$ (T2CON.0). An 3-channel input capture module makes Timer 2 detect and measure the width or period of input pulses. The results of 3 input captures are stores in C0H and C0L, C1H and C1L, C2H and C2L individually. The clock source of Timer 2 is from the system clock pre-scaled by a clock divider with 8 different scales for wide field application. The clock is enabled when TR2 (T2CON.2) is 1, and disabled when TR2 is 0. The following registers are related to Timer 2 function.



[1] Once CAPCR and LDEN are both set, an input capture event only clears TH2 and TL2 without reloading RCMP2H and RCMP2L contents.

Figure 9-1. Timer 2 Block Diagram

T2CON – Timer 2 Control

7	6	5	4	3	2	1	0
TF2	-	-	-	-	TR2	-	$\overline{\text{——}}$
R/W	-	-	-	-	R/W	-	R/W

Address: C8H Reset value: 0000 0000b

Bit	Name	Description
7	TF2	**Timer 2 overflow flag** This bit is set when Timer 2 overflows or a compare match occurs. If the Timer 2 interrupt and the global interrupt are enable, setting this bit will make CPU execute Timer 2 interrupt service routine. This bit is not automatically cleared via hardware and should be cleared via software.
2	TR2	**Timer 2 run control** 0 = Timer 2 Disabled. Clearing this bit will halt Timer 2 and the current count will be preserved in TH2 and TL2. 1 = Timer 2 Enabled.
0	$\overline{\text{——}}$	**Timer 2 compare or auto-reload mode select** This bit selects Timer 2 functioning mode. 0 = Auto-reload mode. 1 = Compare mode.

T2MOD – Timer 2 Mode

7	6	5	4	3	2	1	0
LDEN	T2DIV[2:0]			CAPCR	CMPCR	LDTS[1:0]	
R/W	R/W			R/W	R/W	R/W	

Address: C9H Reset value: 0000 0000b

Bit	Name	Description
7	LDEN	**Enable auto-reload** 0 = Reloading RCMP2H and RCMP2L to TH2 and TL2 Disabled. 1 = Reloading RCMP2H and RCMP2L to TH2 and TL2 Enabled.
6:4	T2DIV[2:0]	**Timer 2 clock divider** 000 = Timer 2 clock divider is 1/1. 001 = Timer 2 clock divider is 1/4. 010 = Timer 2 clock divider is 1/16. 011 = Timer 2 clock divider is 1/32. 100 = Timer 2 clock divider is 1/64. 101 = Timer 2 clock divider is 1/128. 110 = Timer 2 clock divider is 1/256. 111 = Timer 2 clock divider is 1/512.
3	CAPCR	**Capture auto-clear** This bit is valid only under Timer 2 auto-reload mode. It enables hardware auto-clearing TH2 and TL2 counter registers after they have been transferred in to RCMP2H and RCMP2L while a capture event occurs. 0 = Timer 2 continues counting when a capture event occurs. 1 = Timer 2 value is auto-cleared as 0000H when a capture event occurs.
2	CMPCR	**Compare match auto-clear** This bit is valid only under Timer 2 compare mode. It enables hardware auto-clearing TH2 and TL2 counter registers after a compare match occurs. 0 = Timer 2 continues counting when a compare match occurs. 1 = Timer 2 value is auto-cleared as 0000H when a compare match occurs.

Bit	Name	Description
1:0	LDTS[1:0]	**Auto-reload trigger select** These bits select the reload trigger event. 00 = Reload when Timer 2 overflows. 01 = Reload when input capture 0 event occurs. 10 = Reload when input capture 1 event occurs. 11 = Reload when input capture 2 event occurs.

RCMP2L – Timer 2 Reload/Compare Low Byte

7	6	5	4	3	2	1	0
RCMP2L[7:0]							
R/W							

Address: CAH Reset value: 0000 0000b

Bit	Name	Description
7:0	RCMP2L[7:0]	**Timer 2 reload/compare low byte** This register stores the low byte of compare value when Timer 2 is configured in compare mode. Also it holds the low byte of the reload value in auto-reload mode.

RCMP2H – Timer 2 Reload/Compare High Byte

7	6	5	4	3	2	1	0
RCMP2H[7:0]							
R/W							

Address: CBH Reset value: 0000 0000b

Bit	Name	Description
7:0	RCMP2H[7:0]	**Timer 2 reload/compare high byte** This register stores the high byte of compare value when Timer 2 is configured in compare mode. Also it holds the high byte of the reload value in auto-reload mode.

TL2 – Timer 2 Low Byte

7	6	5	4	3	2	1	0
TL2[7:0]							
R/W							

Address: CCH, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	TL2[7:0]	**Timer 2 low byte** The TL2 register is the low byte of the 16-bit counting register of Timer 2.

TH2 – Timer 2 High Byte

7	6	5	4	3	2	1	0
TH2[7:0]							
R/W							

Address: CDH, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	TH2[7:0]	**Timer 2 high byte** The TH2 register is the high byte of the 16-bit counting register of Timer 2.

Note that the TH2 and TL2 are accessed separately. It is strongly recommended that user stops Timer 2 temporally by clearing TR2 bit before reading from or writing to TH2 and TL2. The free-running reading or writing may cause unpredictable result.

9.1 Auto-Reload Mode

The Timer 2 is configured as auto-reload mode by clearing ____. In this mode RCMP2H and RCMP2L registers store the reload value. The contents in RCMP2H and RCMP2L transfer into TH2 and TL2 once the auto-reload event occurs if setting LDEN bit. The event can be the Timer 2 overflow or one of the triggering event on any of enabled input capture channel depending on the LDTS[1:0] (T2MOD[1:0]) selection. Note that once CAPCR (T2MOD.3) is set, an input capture event only clears TH2 and TL2 without reloading RCMP2H and RCMP2L contents.

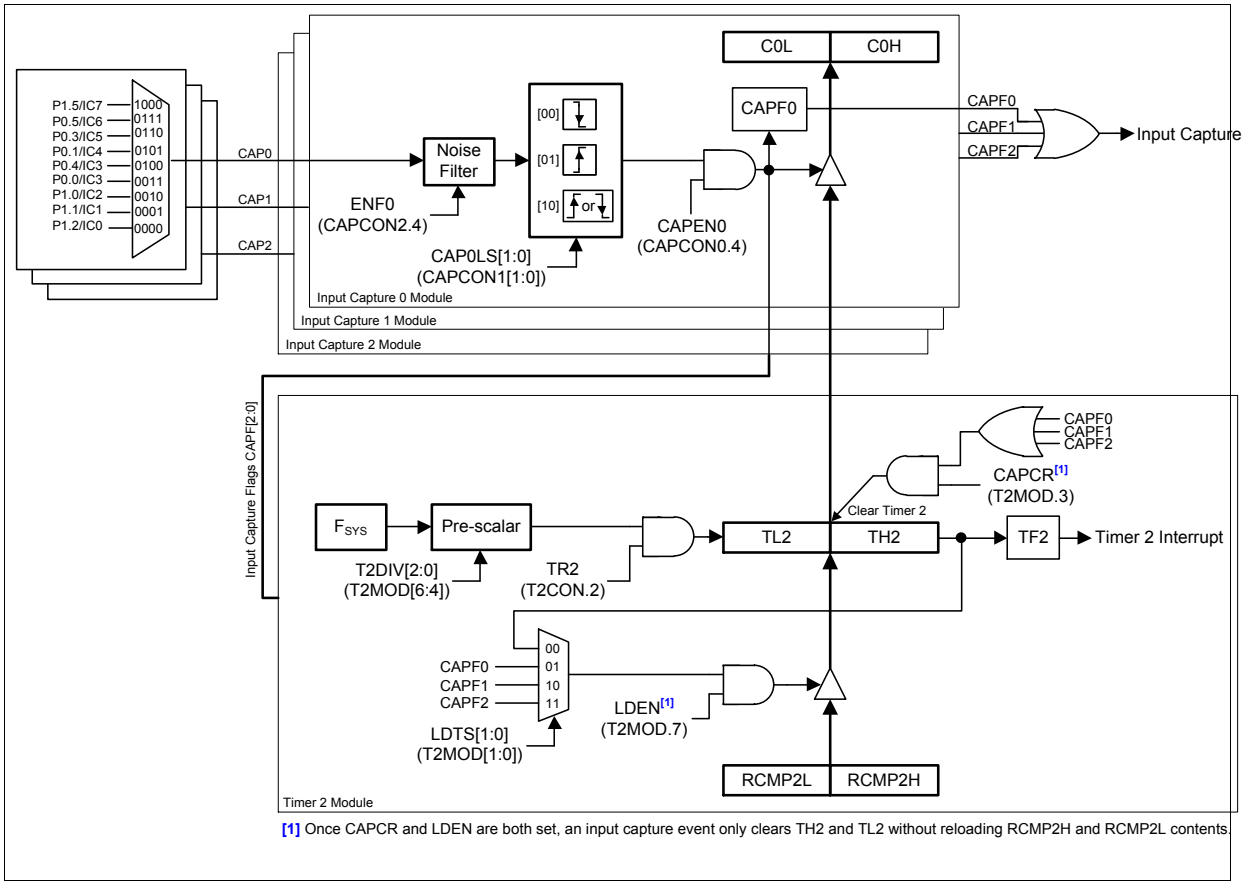


Figure 9-2. Timer 2 Auto-Reload Mode and Input Capture Module Functional Block Diagram

9.2 Compare Mode

Timer 2 can also be configured as the compare mode by setting ____. In this mode RCMP2H and RCMP2L registers serve as the compare value registers. As Timer 2 up counting, TH2 and TL2 match RCMP2H and RCMP2L, TF2 (T2CON.7) will be set by hardware to indicate a compare match event.

Setting CMPCR (T2MOD.2) makes the hardware to clear Timer 2 counter as 0000H automatically after a compare match has occurred.

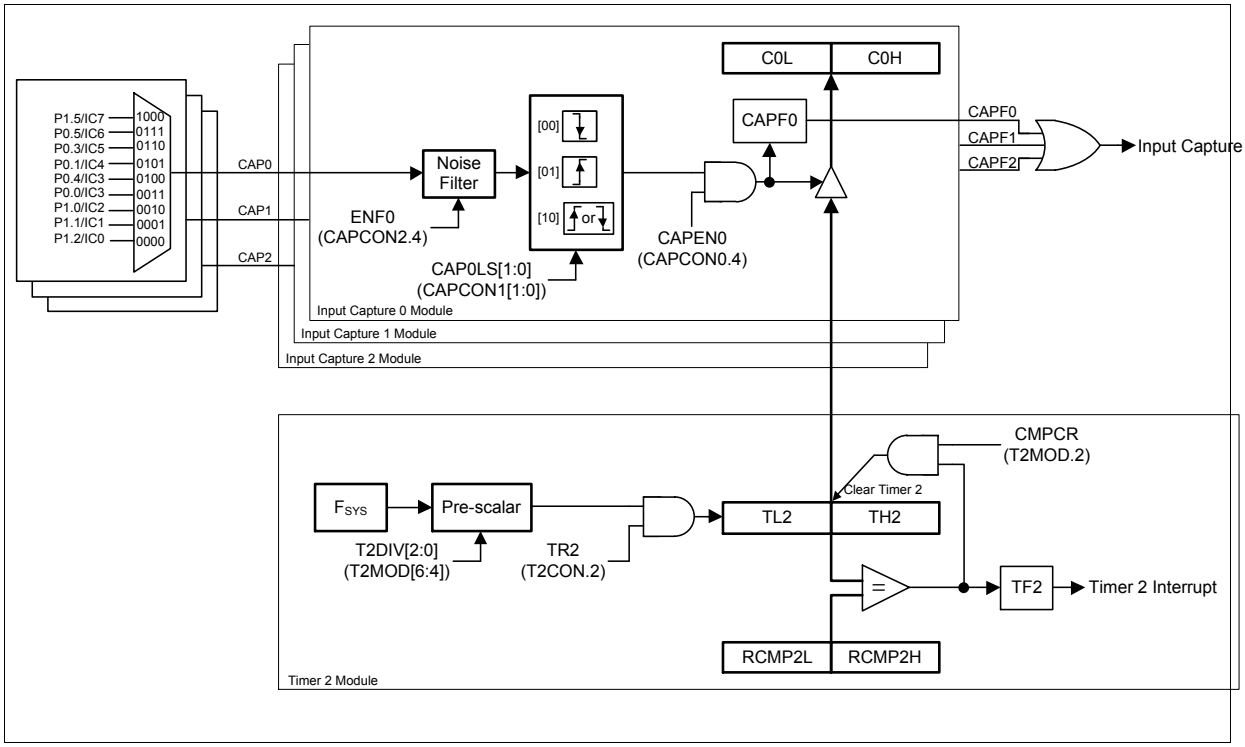


Figure 9-3. Timer 2 Compare Mode and Input Capture Module Functional Block Diagram

9.3 Input Capture Module

The input capture module along with Timer 2 implements the input capture function. The input capture module is configured through CAPCON0~2 registers. The input capture module supports 3-channel inputs (CAP0, CAP1, and CAP2) that share 9 I/O pins (P1.5, P1[2:0], P0.0, P0.1 and P0[5:3]). The pin mux select through CAPCON3 and CAPCON4. Each input channel consists its own noise filter, which is enabled via setting ENF0~2 (CAPCON2[6:4]). It filters input glitches smaller than four system clock cycles. Input capture channels has their own independent edge detector but share the unique Timer 2. Each trigger edge detector is selected individually by setting corresponding bits in CAPCON1. It supports positive edge capture, negative edge capture, or any edge capture. Each input capture channel has to set its own enabling bit CAPEN0~2 (CAPCON0[6:4]) before use.

While input capture channel is enabled and the selected edge trigger occurs, the content of the free running Timer 2 counter, TH2 and TL2, will be captured, transferred, and stored into the capture registers CnH and CnL. The edge triggering also causes CAPFn (CAPCON0.n) set by hardware. The interrupt will also generate if the ECAP (EIE.2) and EA bit are both set. For three input capture flags share the same interrupt vector, user should check CAPFn to confirm which channel comes the input capture edge. These flags should be cleared by software.

The bit CAPCR (CAPCON2.3) benefits the implement of period calculation. Setting CAPCR makes the hardware clear Timer 2 as 0000H automatically after the value of TH2 and TL2 have been captured after an input capture edge event occurs. It eliminates the routine software overhead of writing 16-bit counter or an arithmetic subtraction.

CAPCON0 – Input Capture Control 0

7	6	5	4	3	2	1	0
-	CAPEN2	CAPEN1	CAPEN0	-	CAPF2	CAPF1	CAPF0
-	R/W	R/W	R/W	-	R/W	R/W	R/W

Address: 92H Reset value: 0000 0000b

Bit	Name	Description
6	CAPEN2	**Input capture 2 enable** 0 = Input capture channel 2 Disabled. 1 = Input capture channel 2 Enabled.
5	CAPEN1	**Input capture 1 enable** 0 = Input capture channel 1 Disabled. 1 = Input capture channel 1 Enabled.
4	CAPEN0	**Input capture 0 enable** 0 = Input capture channel 0 Disabled. 1 = Input capture channel 0 Enabled.
2	CAPF2	**Input capture 2 flag** This bit is set by hardware if the determined edge of input capture 2 occurs. This bit should cleared by software.
1	CAPF1	**Input capture 1 flag** This bit is set by hardware if the determined edge of input capture 1 occurs. This bit should cleared by software.
0	CAPF0	**Input capture 0 flag** This bit is set by hardware if the determined edge of input capture 0 occurs. This bit should cleared by software.

CAPCON1 – Input Capture Control 1

7	6	5	4	3	2	1	0
-	-	CAP2LS[1:0]		CAP1LS[1:0]		CAP0LS[1:0]	
-	-	R/W		R/W		R/W	

Address: 93H Reset value: 0000 0000b

Bit	Name	Description
5:4	CAP2LS[1:0]	**Input capture 2 level select** 00 = Falling edge. 01 = Rising edge. 10 = Either Rising or falling edge. 11 = Reserved.
3:2	CAP1LS[1:0]	**Input capture 1 level select** 00 = Falling edge. 01 = Rising edge. 10 = Either Rising or falling edge. 11 = Reserved.
1:0	CAP0LS[1:0]	**Input capture 0 level select** 00 = Falling edge. 01 = Rising edge. 10 = Either Rising or falling edge. 11 = Reserved.

CAPCON2 – Input Capture Control 2

7	6	5	4	3	2	1	0
-	ENF2	ENF1	ENF0	-	-	-	-
-	R/W	R/W	R/W	-	-	-	-

Address: 94H Reset value: 0000 0000b

Bit	Name	Description
6	ENF2	**Enable noise filer on input capture 2** 0 = Noise filter on input capture channel 2 Disabled. 1 = Noise filter on input capture channel 2 Enabled.
5	ENF1	**Enable noise filer on input capture 1** 0 = Noise filter on input capture channel 1 Disabled. 1 = Noise filter on input capture channel 1 Enabled.
4	ENF0	**Enable noise filer on input capture 0** 0 = Noise filter on input capture channel 0 Disabled. 1 = Noise filter on input capture channel 0 Enabled.

C0L – Capture 0 Low Byte

7	6	5	4	3	2	1	0
C0L[7:0]							
R/W							

Address: E4H Reset value: 0000 0000b

Bit	Name	Description
7:0	C0L[7:0]	**Input capture 0 result low byte** The C0L register is the low byte of the 16-bit result captured by input capture 0.

C0H – Capture 0 High Byte

7	6	5	4	3	2	1	0
C0H[7:0]							
R/W							

Address: E5H Reset value: 0000 0000b

Bit	Name	Description
7:0	C0H[7:0]	**Input capture 0 result high byte** The C0H register is the high byte of the 16-bit result captured by input capture 0.

C1L – Capture 1 Low Byte

7	6	5	4	3	2	1	0
C1L[7:0]							
R/W							

Address: E6H Reset value: 0000 0000b

Bit	Name	Description
7:0	C1L[7:0]	**Input capture 1 result low byte** The C1L register is the low byte of the 16-bit result captured by input capture 1.

C1H – Capture 1 High Byte

7	6	5	4	3	2	1	0
C1H[7:0]							
R/W							

Address: E7H Reset value: 0000 0000b

Bit	Name	Description
7:0	C1H[7:0]	**Input capture 1 result high byte** The C1H register is the high byte of the 16-bit result captured by input capture 1.

C2L – Capture 2 Low Byte

7	6	5	4	3	2	1	0
C2L[7:0]							
R/W							

Address: EDH Reset value: 0000 0000b

Bit	Name	Description
7:0	C2L[7:0]	**Input capture 2 result low byte** The C2L register is the low byte of the 16-bit result captured by input capture 2.

C2H – Capture 2 High Byte

7	6	5	4	3	2	1	0
C2H[7:0]							
R/W							

Address: EEH Reset value: 0000 0000b

Bit	Name	Description
7:0	C2H[7:0]	**Input capture 2 result high byte** The C2H register is the high byte of the 16-bit result captured by input capture 2.

CAPCON3 – Input Capture Control 3

7	6	5	4	3	2	1	0
CAP13	CAP12	CAP11	CAP10	CAP03	CAP02	CAP01	CAP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F1H Reset value: 0000 0000b

Bit	Name	Description
[7:4]	CAP1[3:0]	**Input capture channel 1 input pin select** 0000 = P1.2/IC0 0001 = P1.1/IC1 0010 = P1.0/IC2 0011 = P0.0/IC3 0100 = P0.4/IC3 0101 = P0.1/IC4 0110 = P0.3/IC5 0111 = P0.5/IC6 1000 = P1.5/IC7 others = P1.2/IC0
[3:0]	CAP0[3:0]	**Input capture channel 0 input pin select** 0000 = P1.2/IC0 0001 = P1.1/IC1 0010 = P1.0/IC2 0011 = P0.0/IC3 0100 = P0.4/IC3 0101 = P0.1/IC4 0110 = P0.3/IC5 0111 = P0.5/IC6 1000 = P1.5/IC7 others = P1.2/IC0

CAPCON4 – Input Capture Control 4

7	6	5	4	3	2	1	0
-	-	-	-	CAP23	CAP22	CAP21	CAP20
-	-	-	-	R/W	R/W	R/W	R/W

Address: F2H Reset value: 0000 0000b

Bit	Name	Description
[3:0]	CAP2[3:0]	**Input capture channel 2 input pin select** 0000 = P1.2/IC0 0001 = P1.1/IC1 0010 = P1.0/IC2 0011 = P0.0/IC3 0100 = P0.4/IC3 0101 = P0.1/IC4 0110 = P0.3/IC5 0111 = P0.5/IC6 1000 = P1.5/IC7 others = P1.2/IC0

10. TIMER 3

Timer 3 is implemented simply as a 16-bit auto-reload, up-counting timer. The user can select the pre-scale with T3PS[2:0] (T3CON[2:0]) and fill the reload value into RH3 and RL3 registers to determine its overflow rate. User then can set TR3 (T3CON.3) to start counting. When the counter rolls over FFFFH, TF3 (T3CON.4) is set as 1 and a reload is generated and causes the contents of the RH3 and RL3 registers to be reloaded into the internal 16-bit counter. If ET3 (EIE1.1) is set as 1, Timer 3 interrupt service routine will be served. TF3 is auto-cleared by hardware after entering its interrupt service routine.

Timer 3 can also be the baud rate clock source of both UARTs. For details, please see Section 13.5 "Baud Rate" on page 127.

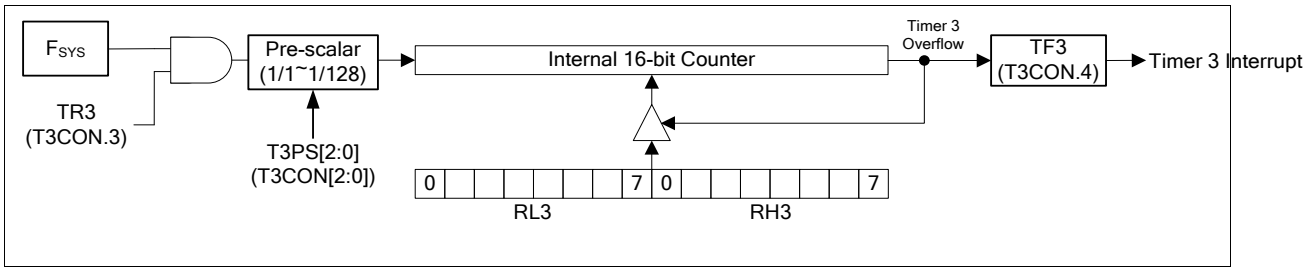


Figure 10-1. Timer 3 Block Diagram

T3CON – Timer 3 Control

7	6	5	4	3	2	1	0
SMOD_1	SMOD0_1	BRCK	TF3	TR3	T3PS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: C4H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
4	TF3	**Timer 3 overflow flag** This bit is set when Timer 3 overflows. It is automatically cleared by hardware when the program executes the Timer 3 interrupt service routine. This bit can be set or cleared by software.
3	TR3	**Timer 3 run control** 0 = Timer 3 is halted. 1 = Timer 3 starts running. Note that the reload registers RH3 and RL3 can only be written when Timer 3 is halted (TR3 bit is 0). If any of RH3 or RL3 is written if TR3 is 1, result is unpredictable.

Bit	Name	Description
2:0	T3PS[2:0]	**Timer 3 pre-scalar** These bits determine the scale of the clock divider for Timer 3. 000 = 1/1. 001 = 1/2. 010 = 1/4. 011 = 1/8. 100 = 1/16. 101 = 1/32. 110 = 1/64. 111 = 1/128.

RL3 – Timer 3 Reload Low Byte

7	6	5	4	3	2	1	0
RL3[7:0]							
R/W							

Address: C5H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	RL3[7:0]	**Timer 3 reload low byte** It holds the low byte of the reload value of Timer 3.

RH3 – Timer 3 Reload High Byte

7	6	5	4	3	2	1	0
RH3[7:0]							
R/W							

Address: C6H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7:0	RH3[7:0]	**Timer 3 reload high byte** It holds the high byte of the reload value of Time 3.

11. WATCHDOG TIMER (WDT)

The N76E003 provides one Watchdog Timer (WDT). It can be configured as a time-out reset timer to reset whole device. Once the device runs in an abnormal status or hangs up by outward interference, a WDT reset recover the system. It provides a system monitor, which improves the reliability of the system. Therefore, WDT is especially useful for system that is susceptible to noise, power glitches, or electrostatic discharge. The WDT also can be configured as a general purpose timer, of which the periodic interrupt serves as an event timer or a durational system supervisor in a monitoring system, which is able to operate during Idle or Power-down mode. WDTEN[3:0] (CONFIG4[7:4]) initialize the WDT to operate as a time-out reset timer or a general purpose timer.

CONFIG4

7	6	5	4	3	2	1	0
WDTEN[3:0]				-	-	-	-
R/W				-	-	-	-

Factory default value: 1111 1111b

Bit	Name	Description
7:4	WDTEN[3:0]	**WDT enable** This field configures the WDT behavior after MCU execution. 1111 = WDT is Disabled. WDT can be used as a general purpose timer via software control. 0101 = WDT is Enabled as a time-out reset timer and it stops running during Idle or Power-down mode. Others = WDT is Enabled as a time-out reset timer and it keeps running during Idle or Power-down mode.

The WDT is implemented with a set of divider that divides the low-speed internal oscillator clock nominal 10 kHz. The divider output is selectable and determines the time-out interval. When the time-out interval is fulfilled, it will wake the system up from Idle or Power-down mode and an interrupt event will occur if WDT interrupt is enabled. If WDT is initialized as a time-out reset timer, a system reset will occur after a period of delay if without any software action.

WDCON – Watchdog Timer Control (TA protected)

7	6	5	4	3	2	1	0
WDTR	WDCLR	WDTF	WIDPD	WDTRF[1]	WDPS[2:0][2]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: AAH Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
7	WDTR	**WDT run** This bit is valid only when control bits in WDTEN[3:0] (CONFIG4[7:4]) are all 1. At this time, WDT works as a general purpose timer. 0 = WDT Disabled. 1 = WDT Enabled. The WDT counter starts running.

Bit	Name	Description
6	WDCLR	**WDT clear** Setting this bit will reset the WDT count to 00H. It puts the counter in a known state and prohibit the system from unpredictable reset. The meaning of writing and reading WDCLR bit is different. Writing: 0 = No effect. 1 = Clearing WDT counter. Reading: 0 = WDT counter is completely cleared. 1 = WDT counter is not yet cleared.
5	WDTF	**WDT time-out flag** This bit indicates an overflow of WDT counter. This flag should be cleared by software.
4	WIDPD	**WDT running in Idle or Power-down mode** This bit is valid only when control bits in WDTEN[3:0] (CONFIG4[7:4]) are all 1. It decides whether WDT runs in Idle or Power-down mode when WDT works as a general purpose timer. 0 = WDT stops running during Idle or Power-down mode. 1 = WDT keeps running during Idle or Power-down mode.
3	WDTRF	**WDT reset flag** When the CPU is reset by WDT time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software after reset.
2:0	WDPS[2:0]	**WDT clock pre-scalar select** These bits determine the pre-scale of WDT clock from 1/1 through 1/256. See Table 11-1. The default is the maximum pre-scale value.

[1] WDTRF will be cleared after power-on reset, be set after WDT reset, and remains unchanged after any other resets.

[2] WDPS[2:0] are all set after power-on reset and keep unchanged after any reset other than power-on reset.

The Watchdog time-out interval is determined by the formula $\frac{1}{F_{LIRC} \times clock\,divider\,scalar} \times 64$, where F_{LIRC} is the frequency of internal 10 kHz oscillator. The following table shows an example of the Watchdog time-out interval with different pre-scales.

Table 11-1. Watchdog Timer-out Interval Under Different Pre-scalars

WDPS.2	WDPS.1	WDPS.0	Clock Divider Scale	Watchdog Time-out Interval (F_{LIRC} ~= 10 kHz)
0	0	0	1/1	6.40 ms
0	0	1	1/4	25.60 ms
0	1	0	1/8	51.20 ms
0	1	1	1/16	102.40 ms
1	0	0	1/32	204.80 ms
1	0	1	1/64	409.60 ms
1	1	0	1/128	819.20 ms
1	1	1	1/256	1.638 s

11.1 Time-Out Reset Timer

When the CONFIG bits WDTEN[3:0] (CONFIG4[7:4]) is not FH, the WDT is initialized as a time-out reset timer. If WDTEN[3:0] is not 5H, the WDT is allowed to continue running after the system enters Idle or Power-down mode. Note that when WDT is initialized as a time-out reset timer, WDTR and WIDPD has no function.

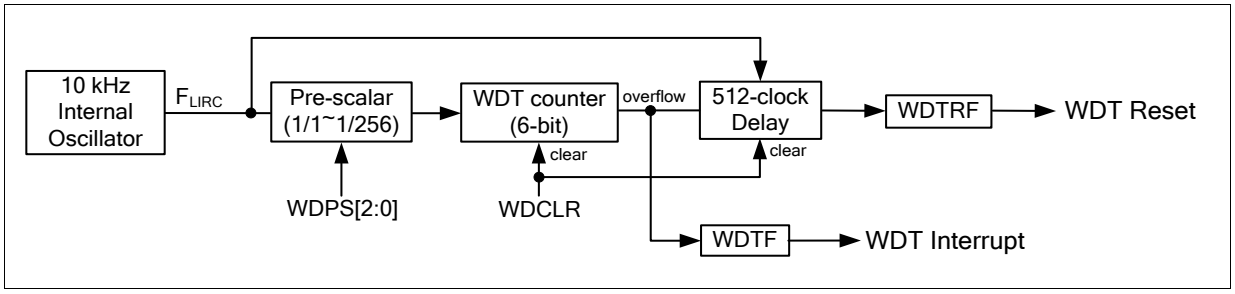


Figure 11-1. WDT as A Time-Out Reset Timer

After the device is powered and it starts to execute software code, the WDT starts counting simultaneously. The time-out interval is selected by the three bits WDPS[2:0] (WDCON[2:0]). When the selected time-out occurs, the WDT will set the interrupt flag WDTF (WDCON.5). If the WDT interrupt enable bit EWDT (EIE.4) and global interrupt enable EA are both set, the WDT interrupt routine will be executed. Meanwhile, an additional 512 clocks of the low-speed internal oscillator delays to expect a counter clearing by setting WDCLR to avoid the system reset by WDT if the device operates normally. If no counter reset by writing 1 to WDCLR during this 512-clock period, a WDT reset will happen. Setting WDCLR bit is used to clear the counter of the WDT. This bit is self-cleared for user monitoring it. Once a reset due to WDT occurs, the WDT reset flag WDTRF (WDCON.3) will

be set. This bit keeps unchanged after any reset other than a power-on reset. User may clear WDTRF via software. Note that all bits in WDCON require timed access writing.

NOTICE: WDT counter has been specially taken care. The hardware automatically clears WDT counter and pre-scalar value after :

(1) Entering into or being woken-up from Idle or Power Down mode
(2) Any resets. It prevents unconscious system reset.

The main application of the WDT with time-out reset enabling is for the system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, CPU may begin to execute erroneous codes and operate in an unpredictable state. If this is left unchecked the entire system may crash. Using the WDT during software development requires user to select proper "Feeding Dog" time by clearing the WD counter. By inserting the instruction of setting WDCLR, it allows the code to run without any WDT reset. However If any erroneous code executes by any interference, the instructions to clear the WDT counter will not be executed at the required instants. Thus the WDT reset will occur to reset the system state from an erroneously executing condition and recover the system.

11.2 General Purpose Timer

There is another application of the WDT, which is used as a simple, long period timer. When the CONFIG bits WDTEN[3:0] (CONFIG4[7:4]) is FH, the WDT is initialized as a general purpose timer. In this mode, WDTR and WIDPD are fully accessed via software.

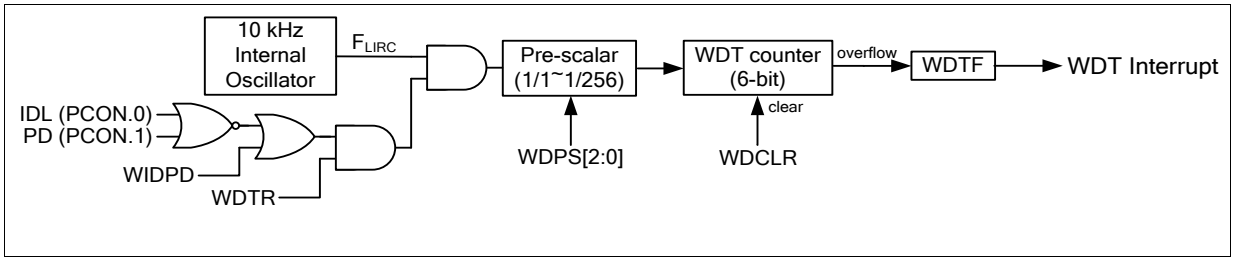


Figure 11-2. Watchdog Timer Block Diagram

The WDT starts running by setting WDTR as 1 and halts by clearing WDTR as 0. The WDTF flag will be set while the WDT completes the selected time interval. The software polls the WDTF flag to detect a time-out. An interrupt will occur if the individual interrupt EWDT (EIE.4) and global interrupt enable EA is set. WDT will continue counting. User should clear WDTF and wait for the next overflow by polling WDTF flag or waiting for the interrupt occurrence.

In some application of low power consumption, the CPU usually stays in Idle mode when nothing needs to be served to save power consumption. After a while the CPU will be woken up to check if

anything needs to be served at an interval of programmed period implemented by Timer 0~3. However, the current consumption of dle mode still keeps at a “mA” level. o further reducing the current consumption to “mA” level, the PU should stay in Power-down mode when nothing needs to be served, and has the ability of waking up at a programmable interval. The N76E003 is equipped with this useful function by WDT waking up. It provides a very low power internal oscillator 10 kHz as the clock source of the WDT. It is also able to count under Power-down mode and wake CPU up. The demo code to accomplish this feature is shown below.

For Example:

```
        ORG    0000H
        LJMP   START

        ORG    0053H
        LJMP   WDT_ISR

        ORG    0100H
;*****************************************************************
;WDT interrupt service routine
;*****************************************************************
WDT_ISR:
        CLR    EA
        MOV    TA,#0AAH
        MOV    TA,#55H
        ANL    WDCON,#11011111B    ;clear WDT interrupt flag
        SETB   EA
        RETI

;*****************************************************************
;Start here
;*****************************************************************
START:
        MOV    TA,#0AAH
        MOV    TA,#55H
        ORL    WDCON,#00010111B    ;choose  interval  length  and  enable  WDT  running
during                                ;Power-down
        SETB   EWDT                ;enable WDT interrupt
        SETB   EA

        MOV    TA,#0AAH
        MOV    TA,#55H
        ORL    WDCON,#10000000B    ; WDT run

;*****************************************************************
;Enter Power-down mode
;*****************************************************************
LOOP:
        ORL    PCON,#02H
        LJMP   LOOP
```

12. SELF WAKE-UP TIMER (WKT)

The N76E003 has a dedicated Self Wake-up Timer (WKT), which serves for a periodic wake-up timer in low power mode or for general purpose timer. WKT remains counting in Idle or Power-down mode. When WKT is being used as a wake-up timer, a start of WKT can occur just prior to entering a power management mode. WKT has one clock source, internal 10 kHz. Note that the system clock frequency must be twice over WKT clock. If WKT starts counting, the selected clock source will remain active once the device enters Idle or Power-down mode. Note that the selected clock source of WKT will not automatically enabled along with WKT configuration. User should manually enable the selected clock source and waiting for stability to ensure a proper operation.

The WKT is implemented simply as a 8-bit auto-reload, up-counting timer with pre-scale 1/1 to 1/2048 selected by WKPS[2:0] (WKCON[2:0]). User fills the reload value into RWK register to determine its overflow rate. The WKTR (WKCON.3) can be set to start counting. When the counter rolls over FFH, WKTF (WKCON.4) is set as 1 and a reload is generated and causes the contents of the RWK register to be reloaded into the internal 8-bit counter. If EWKT (EIE1.2) is set as 1, WKT interrupt service routine will be served.

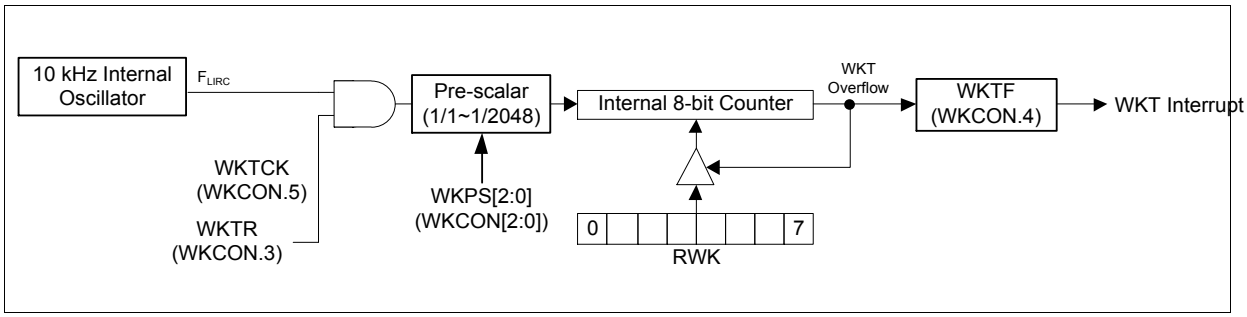


Figure 12-1. Self Wake Up Timer Block Diagram

WKCON – Self Wake-up Timer Control

7	6	5	4	3	2	1	0
-	-	-	WKTF	WKTR	WKPS[2:0]		
-	-	-	R/W	R/W	R/W		

Address: 8FH Reset value: 0000 0000b

Bit	Name	Description
5	-	**Reserved**
4	WKTF	**WKT overflow flag** This bit is set when WKT overflows. If the WKT interrupt and the global interrupt are enabled, setting this bit will make CPU execute WKT interrupt service routine. This bit is not automatically cleared via hardware and should be cleared via software.

Bit	Name	Description
3	WKTR	**WKT run control** 0 = WKT is halted. 1 = WKT starts running. Note that the reload register RWK can only be written when WKT is halted (WKTR bit is 0). If WKT is written while WKTR is 1, result is unpredictable.
2:0	WKPS[2:0]	**WKT pre-scalar** These bits determine the pre-scale of WKT clock. 000 = 1/1. 001 = 1/4. 010 = 1/16. 011 = 1/64. 100 = 1/256. 101 = 1/512. 110 = 1/1024. 111 = 1/2048.

RWK – Self Wake-up Timer Reload Byte

7	6	5	4	3	2	1	0
RWK[7:0]							
R/W							

Address: 86H Reset value: 0000 0000b

Bit	Name	Description
7:0	RWK[7:0]	**WKT reload byte** It holds the 8-bit reload value of WKT. Note that RWK should not be FFH if the pre-scale is 1/1 for implement limitation.

13. SERIAL PORT (UART)

The N76E003 includes two enhanced full duplex serial ports enhanced with automatic address recognition and framing error detection. As control bits of these two serial ports are implemented the same, the bit names (including interrupt enabling or priority setting bits) end with "_" (e.g. O _1) to indicate serial port 1 control bits for making a distinction between these two serial ports. Generally speaking, in the following contents, there will not be any reference to serial port 1, but only to serial port 0.

Each serial port supports one synchronous communication mode, Mode 0, and three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter), Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receiving-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The receiving and transmitting registers are both accessed at SBUF. Writing to SBUF loads the transmitting register, and reading SBUF accesses a physically separate receiving register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register. Note that before serial port function works, the port latch bits of P0.7 and P0.6 (for RXD and TXD pins) or P0.2 and P1.6 (for RXD_1 and TXD_1 pins) have to be set to 1. For application flexibility, TXD and RXD pins of serial port 0 can be exchanged by UART0PX (AUXR1.2).

SCON – Serial Port Control (Bit-addressable)

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 98H Reset value: 0000 0000b

Bit	Name	Description
7	SM0/FE	**Serial port mode select**
6	SM1	SMOD0 (PCON.6) = 0: See Table 13-1. Serial Port 0 Mode Description for details. SMOD0 (PCON.6) = 1: SM0/FE bit is used as frame error (FE) status flag. It is cleared by software. 0 = Frame error (FE) did not occur. 1 = Frame error (FE) occurred and detected.

Bit	Name	Description
5	SM2	**Multiprocessor communication mode enable** The function of this bit is dependent on the serial port 0 mode. Mode 0: This bit select the baud rate between F_{SYS}/12 and F_{SYS}/2. 0 = The clock runs at F_{SYS}/12 baud rate. It maintains standard 8051 compatibility. 1 = The clock runs at F_{SYS}/2 baud rate for faster serial communication. Mode 1: This bit checks valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is valid only when the received stop bit is logic 1 and the received data matches “Given” or “Broadcast” address. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is valid only when the received 9th bit is logic 1 and the received data matches “Given” or “Broadcast” address.
4	REN	**Receiving enable** 0 = Serial port 0 reception Disabled. 1 = Serial port 0 reception Enabled in Mode 1,2, or 3. In Mode 0, reception is initiated by the condition REN = 1 and RI = 0.
3	TB8	**9th transmitted bit** This bit defines the state of the 9th transmission bit in serial port 0 Mode 2 or 3. It is not used in Mode 0 or 1.
2	RB8	**9th received bit** The bit identifies the logic level of the 9th received bit in serial port 0 Mode 2 or 3. In Mode 1, RB8 is the logic level of the received stop bit. SM2 bit as logic 1 has restriction for exception. RB8 is not used in Mode 0.
1	TI	**Transmission interrupt flag** This flag is set by hardware when a data frame has been transmitted by the serial port 0 after the 8th bit in Mode 0 or the last data bit in other modes. When the serial port 0 interrupt is enabled, setting this bit causes the CPU to execute the serial port 0 interrupt service routine. This bit should be cleared manually via software.
0	RI	**Receiving interrupt flag** This flag is set via hardware when a data frame has been received by the serial port 0 after the 8th bit in Mode 0 or after sampling the stop bit in Mode 1, 2, or 3. SM2 bit as logic 1 has restriction for exception. When the serial port 0 interrupt is enabled, setting this bit causes the CPU to execute to the serial port 0 interrupt service routine. This bit should be cleared manually via software.

SCON_1 – Serial Port 1 Control (bit-addressable)

7	6	5	4	3	2	1	0
SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F8H Reset value: 0000 0000b

Bit	Name	Description
7	SM0_1/FE_1	**Serial port 1 mode select** SMOD0_1 (T3CON.6) = 0: See Table 13-2. Serial Port 1 Mode Description for details. SMOD0_1 (T3CON.6) = 1: SM0_1/FE_1 bit is used as frame error (FE) status flag. It is cleared by software. 0 = Frame error (FE) did not occur. 1 = Frame error (FE) occurred and detected.
6	SM1_1	
5	SM2_1	**Multiprocessor communication mode enable** The function of this bit is dependent on the serial port 1 mode. Mode 0: No effect. Mode 1: This bit checks valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is valid only when the received stop bit is logic 1 and the received data matches “Given” or “Broadcast” address. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is valid only when the received 9th bit is logic 1 and the received data matches “Given” or “Broadcast” address.
4	REN_1	**Receiving enable** 0 = Serial port 1 reception Disabled. 1 = Serial port 1 reception Enabled in Mode 1,2, or 3. In Mode 0, reception is initiated by the condition REN_1 = 1 and RI_1 = 0.
3	TB8_1	**9th transmitted bit** This bit defines the state of the 9th transmission bit in serial port 1 Mode 2 or 3. It is not used in Mode 0 or 1.
2	RB8_1	**9th received bit** The bit identifies the logic level of the 9th received bit in serial port 1 Mode 2 or 3. In Mode 1, RB8_1 is the logic level of the received stop bit. SM2_1 bit as logic 1 has restriction for exception. RB8_1 is not used in Mode 0.
1	TI_1	**Transmission interrupt flag** This flag is set by hardware when a data frame has been transmitted by the serial port 1 after the 8th bit in Mode 0 or the last data bit in other modes. When the serial port 1 interrupt is enabled, setting this bit causes the CPU to execute the serial port 1 interrupt service routine. This bit must be cleared manually via software.

Bit	Name	Description
0	RI_1	**Receiving interrupt flag** This flag is set via hardware when a data frame has been received by the serial port 1 after the 8th bit in Mode 0 or after sampling the stop bit in Mode 1, 2, or 3. SM2_1 bit as logic 1 has restriction for exception. When the serial port 1 interrupt is enabled, setting this bit causes the CPU to execute to the serial port 1 interrupt service routine. This bit must be cleared manually via software.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W

Address: 87H Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
7	SMOD	**Serial port 0 double baud rate enable** Setting this bit doubles the serial port baud rate when UART0 is in Mode 2 or when Timer 1 overflow is used as the baud rate source of UART0 Mode 1 or 3. See Table 13-1. Serial Port 0 Mode Description for details.
6	SMOD0	**Serial port 0 framing error flag access enable** 0 = SCON.7 accesses to SM0 bit. 1 = SCON.7 accesses to FE bit.

T3CON – Timer 3 Control

7	6	5	4	3	2	1	0
SMOD_1	SMOD0_1	BRCK	TF3	TR3	T3PS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: C4H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
7	SMOD_1	**Serial port 1 double baud rate enable** Setting this bit doubles the serial port baud rate when UART1 is in Mode 2. See Table 13-2. Serial Port 1 Mode Description for details.
6	SMOD0_1	**Serial port 1 framing error access enable** 0 = SCON_1.7 accesses to SM0_1 bit. 1 = SCON_1.7 accesses to FE_1 bit.

Table 13-1. Serial Port 0 Mode Description

Mode	SM0	SM1	Description	Frame Bits	Baud Rate
0	0	0	Synchronous	8	F_{SYS} divided by 12 or by 2[1]
1	0	1	Asynchronous	10	Timer 1/Timer 3 overflow rate divided by 32 or 16[2]
2	1	0	Asynchronous	11	F_{SYS} divided by 32 or 64[2]
3	1	1	Asynchronous	11	Timer 1/Timer 3 overflow rate divided by 32 or 16[2]

[1] While SM2 (SCON.5) is logic 1.
[2] While SMOD (PCON.7) is logic 1.

Table 13-2. Serial Port 1 Mode Description

Mode	SM0	SM1	Description	Frame Bits	Baud Rate
0	0	0	Synchronous	8	F_{SYS} divided by 12 or by 2[1]
1	0	1	Asynchronous	10	Timer 3 overflow rate divided by 16
2	1	0	Asynchronous	11	F_{SYS} divided by 32 or 64[2]
3	1	1	Asynchronous	11	Timer 3 overflow rate divided by 16

[1] While SM2_1 (SCON_1.5) is logic 1.
[2] While SMOD_1 (T3CON.7) is logic 1.

SBUF – Serial Port 0 Data Buffer

7	6	5	4	3	2	1	0
SBUF[7:0]							
R/W							

Address: 99H Reset value: 0000 0000b

Bit	Name	Description
7:0	SBUF[7:0]	**Serial port 0 data buffer** This byte actually consists two separate registers. One is the receiving resister, and the other is the transmitting buffer. When data is moved to SBUF, it goes to the transmitting buffer and is shifted for serial transmission. When data is moved from SBUF, it comes from the receiving register. The transmission is initiated through giving data to SBUF.

SBUF_1 – Serial Port 1 Data Buffer

7	6	5	4	3	2	1	0
SBUF_1[7:0]							
R/W							

Address: 9AH Reset value: 0000 0000b

Bit	Name	Description
7:0	SBUF_1[7:0]	**Serial port 1 data buffer** This byte actually consists two separate registers. One is the receiving resister, and the other is the transmitting buffer. When data is moved to SBUF_1, it goes to the transmitting buffer and is shifted for serial transmission. When data is moved from SBUF_1, it comes from the receiving register. The transmission is initiated through giving data to SBUF_1.

AUXR1 – Auxiliary Register 1

7	6	5	4	3	2	1	0
SWRF	RSTPINF	HardF	-	GF2	UART0PX	0	DPS
R/W	R/W	R/W	-	R/W	R/W	R	R/W

Address: A2H Reset value: see Table 6-2. SFR Definitions and Reset Values

Bit	Name	Description
2	UART0PX	**Serial port 0 pin exchange** 0 = Assign RXD to P0.7 and TXD to P0.6 by default. 1 = Exchange RXD to P0.6 and TXD to P0.7. Note that TXD and RXD will exchange immediately once setting or clearing this bit. User should take care of not exchanging pins during transmission or receiving. Or it may cause unpredictable situation and no warning alarms.

13.1 Mode 0

Mode 0 provides synchronous communication with external devices. Serial data enters and exits through RXD pin. TXD outputs the shift clocks. 8-bit frame of data are transmitted or received. Mode 0 therefore provides half-duplex communication because the transmitting or receiving data is via the same data line RXD. The baud rate is enhanced to be selected as $F_{SYS}/12$ if SM2 (SCON.5) is 0 or as $F_{SYS}/2$ if SM2 is 1. Note that whenever transmitting or receiving, the serial clock is always generated by the MCU. Thus any device on the serial port in Mode 0 should accept the MCU as the master. Figure 13-1 shows the associated timing of the serial port in Mode 0.

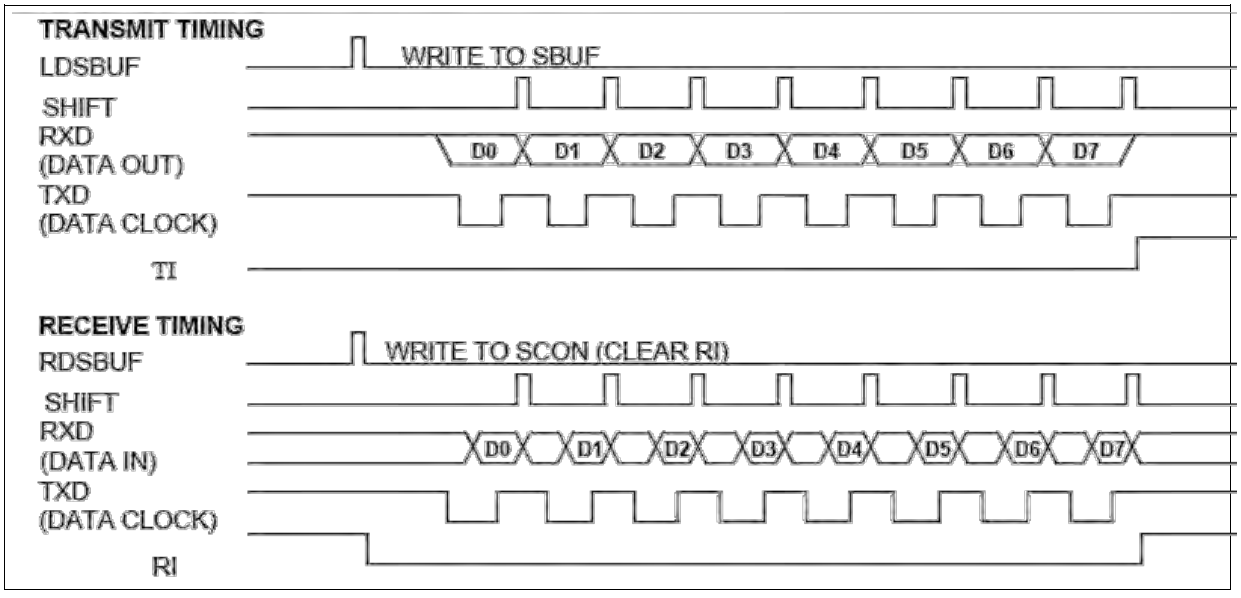


Figure 13-1. Serial Port Mode 0 Timing Diagram

As shown there is one bi-directional data line (RXD) and one shift clock line (TXD). The shift clocks are used to shift data in or out of the serial port controller bit by bit for a serial communication. Data bits enter or emit LSB first. The band rate is equal to the shift clock frequency.

Transmission is initiated by any instruction writes to SBUF. The control block will then shift out the clocks and begin to transfer data until all 8 bits are complete. Then the transmitted flag TI (SCON.1) will be set 1 to indicate one byte transmitting complete.

Reception is initiated by the condition REN (SCON.4) = 1 and RI (SCON.0) = 0. This condition tells the serial port controller that there is data to be shifted in. This process will continue until 8 bits have been received. Then the received flag RI will be set as 1. User can clear RI to triggering the next byte reception.

13.2 Mode 1

Mode 1 supports asynchronous, full duplex serial communication. The asynchronous mode is commonly used for communication with PCs, modems or other similar interfaces. In Mode 1, 10 bits are transmitted through TXD or received through RXD including a start bit (logic 0), 8 data bits (LSB first) and a stop bit (logic 1). The baud rate is determined by the Timer 1. SMOD (PCON.7) setting 1 makes the baud rate double. Figure 13-2 shows the associated timings of the serial port in Mode 1 for transmitting and receiving.

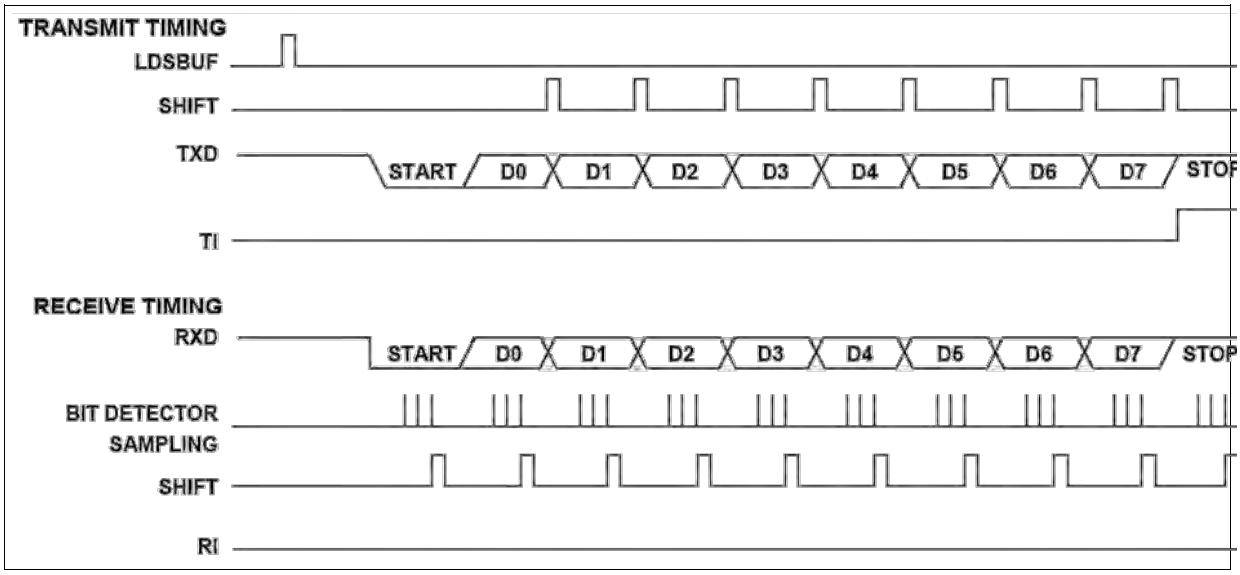


Figure 13-2. Serial Port Mode 1 Timing Diagram

Transmission is initiated by any writing instructions to SBUF. Transmission takes place on TXD pin. First the start bit comes out, the 8-bit data follows to be shifted out and then ends with a stop bit. After the stop bit appears, TI (SCON.1) will be set to indicate one byte transmission complete. All bits are shifted out depending on the rate determined by the baud rate generator.

Once the baud rate generator is activated and REN (SCON.4) is 1, the reception can begin at any time. Reception is initiated by a detected 1-to-0 transition at RXD. Data will be sampled and shifted in

at the selected baud rate. In the midst of the stop bit, certain conditions should be met to load SBUF with the received data:

1. RI (SCON.0) = 0, and

2. Either SM2 (SCON.5) = 0, or the received stop bit = 1 while SM2 = 1 and the received data matches "Given" or "Broadcast" address. (For enhancement function, see 13.7 "Multiprocessor Communication" and 13.8 "Automatic Address Recognition".)

If these conditions are met, then the SBUF will be loaded with the received data, the RB8 (SCON.2) with stop bit, and RI will be set. If these conditions fail, there will be no data loaded and RI will remain 0. After above receiving progress, the serial control will look forward another 1-to-0 transition on RXD pin to start next data reception.

13.3 Mode 2

Mode 2 supports asynchronous, full duplex serial communication. Different from Mode1, there are 11 bits to be transmitted or received. They are a start bit (logic 0), 8 data bits (LSB first), a programmable 9th bit TB8 or RB8 bit and a stop bit (logic 1). The most common use of 9th bit is to put the parity bit in it or to label address or data frame for multiprocessor communication. The baud rate is fixed as 1/32 or 1/64 the system clock frequency depending on SMOD (PCON.7) bit. Figure 13-3 shows the associated timings of the serial port in Mode 2 for transmitting and receiving.

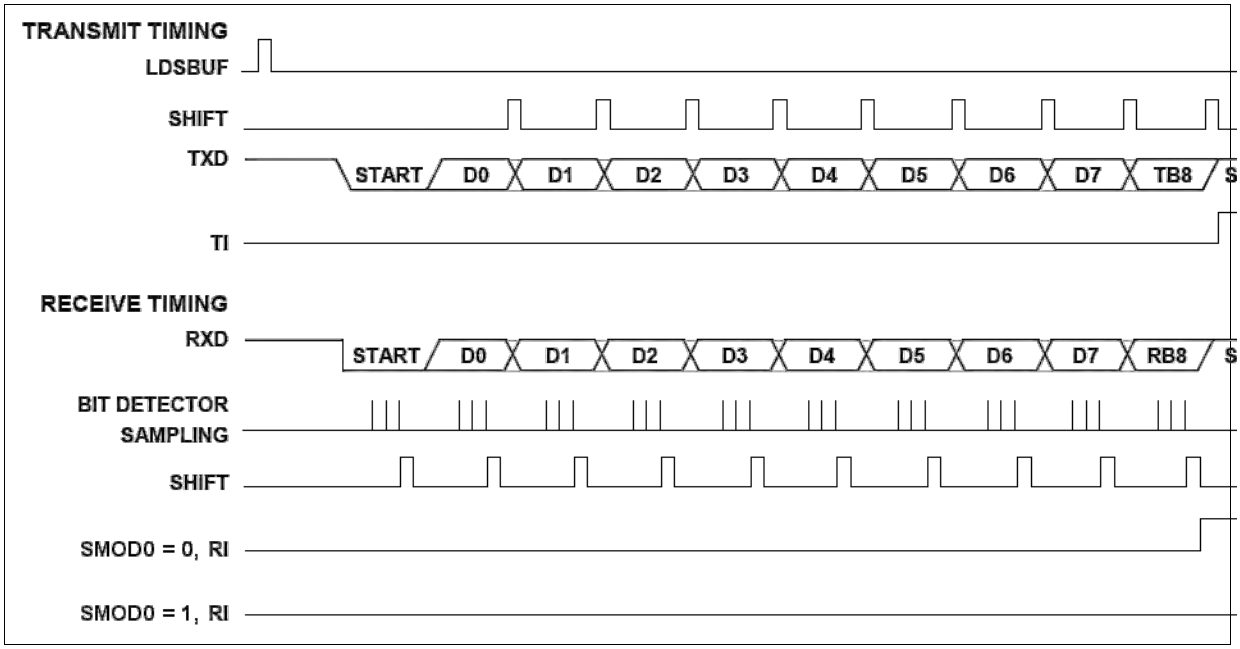


Figure 13-3. Serial Port Mode 2 and 3 Timing Diagram

Transmission is initiated by any writing instructions to SBUF. Transmission takes place on TXD pin. First the start bit comes out, the 8-bit data and bit TB8 (SCON.3) follows to be shifted out and then ends with a stop bit. After the stop bit appears, TI will be set to indicate the transmission complete.

While REN is set, the reception is allowed at any time. A falling edge of a start bit on RXD will initiate the reception progress. Data will be sampled and shifted in at the selected baud rate. In the midst of the stop bit, certain conditions should be met to load SBUF with the received data:

1. RI (SCON.0) = 0, and

2. Either SM2 (SCON.5) = 0, or the received 9th bit = 1 while SM2 = 1 and the received data matches "Given" or "Broadcast" address. (For enhancement function, see 13.7 "Multiprocessor Communication" and 13.8 "Automatic Address Recognition".)

If these conditions are met, the SBUF will be loaded with the received data, the RB8(SCON.2) with the received 9th bit and RI will be set. If these conditions fail, there will be no data loaded and RI will remain 0. After above receiving progress, the serial control will look forward another 1-to-0 transition on RXD pin to start next data reception.

13.4 Mode 3

Mode 3 has the same operation as Mode 2, except its baud rate clock source uses Timer 1 overflows as its baud rate clocks. See Figure 13-3 for timing diagram of Mode 3. It has no difference from Mode 2.

13.5 Baud Rate

The baud rate source and speed for different modes of serial port is quite different from one another. All cases are listed in Table 13-3. The user should calculate the baud rate according to their system configuration.

In Mode 1 or 3, the baud rate clock source of UART0 can be selected from Timer 1 or Timer 3. User can select the baud rate clock source by BRCK (T3CON.5). For UART1, its baud rate clock comes only from Timer 3 as its unique clock source.

T3CON – Timer 3 Control

7	6	5	4	3	2	1	0
SMOD_1	SMOD0_1	BRCK	TF3	TR3	T3PS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: C4H, Page:0 Reset value: 0000 0000b

Bit	Name	Description
5	BRCK	**Serial port 0 baud rate clock source** This bit selects which Timer is used as the baud rate clock source when serial port 0 is in Mode 1 or 3. 0 = Timer 1. 1 = Timer 3.

When using Timer 1 as the baud rate clock source, note that the Timer 1 interrupt should be disabled. Timer 1 itself can be configured for either “ imer” or “ oun ter” operation. It can be in any of its three running modes. However, in the most typical applications, it is configured for “ imer” operation, in the auto-reload mode (Mode 2). If using Timer 3 as the baud rate generator, its interrupt should also be disabled.

Table 13-3. UART Baud Rate Formulas

UART Mode	Baud Rate Clock Source	Baud Rate	Formula Number
0	System clock	$F_{SYS}/12$ or $F_{SYS}/2$ [1]	1
2	System clock	$F_{SYS}/64$ or $F_{SYS}/32$ [2]	2
1 or 3	Timer 1 (only for UART0)[3]	$\frac{2^{SMOD}}{32} \times \frac{F_{SYS}}{12 \times (256 - TH1)}$ or $\frac{2^{SMOD}}{32} \times \frac{F_{SYS}}{256 - TH1}$ [4]	3
	Timer 3 (for UART0)	$\frac{2^{SMOD}}{32} \times \frac{F_{SYS}}{Pre\text{-}scale \times (65536 - \{RH3,RL3\})}$ [5]	4
	Timer 3 (for UART1)	$\frac{1}{16} \times \frac{F_{SYS}}{Pre\text{-}scale \times (65536 - \{RH3,RL3\})}$ [5]	5

[1] SM2 (SCON.5) or SM2_1(SCON_1.5) is set as logic 1.
[2] SMOD (PCON.7) or SMOD_1(T3CON.7) is set as logic 1.
[3] Timer 1 is configured as a timer in auto-reload mode (Mode 2).
[4] T1M (CKCON.4) is set as logic 1. While SMOD is 1, TH1 should not be FFH.
[5] {RH3,RL3} in the formula means $256 \times RH3 + RL3$. While SMOD is 1 and pre-scale is 1/1, {RH3,RL3} should not be FFFFH.

Important: Since the limitation of baud rate generator, **Suggest setting baud rate under 38400 when system timer base 16MHz HIRC value.** Following show the baud rate value table show the deviation upper 38400 baud rate.

HIRC	Target Baud Rate	RHx	RLx	RHx + RLx DEC Value	Actual Baud Rate	Error %
16MHz	2400	0xFE	0x5F	65119	2398.081535	0.079%
	4800	0xFF	0x30	65328	4807.692308	-0.160%
	9600	0xFF	0x98	65432	9615.384615	-0.160%
	19200	0xFF	0xCC	65484	19230.76923	-0.160%
	38400	0xFF	0xE6	65510	38461.53846	-0.160%
	57600	0xFF	0xEF	65519	58823.52941	**-2.124%**
	115200	0xFF	0xF7	65527	111111.1111	**3.549%**

NOTE: RHx and RLx setting value base on baud rate formula 4 (SMOD =1) or 5 .

But In most application the baud rate 115200 is a common setting value. So we provide a special function to modify HIRC to 16.6MHz. then the deviation of baud rate will be reasonable. Following table shows the error value when HIRC and timer base modified.

HIRC	Target Baud Rate	RHx	RLx	RHx + RLx DEC Value	Actual Baud Rate	Error %
16.6MHz	2400	0xFE	0x50	65104	2401.62037	-0.067%
	4800	0xFF	0x28	65320	4803.240741	-0.067%
	9600	0xFF	0x94	65428	9606.481481	-0.067%
	19200	0xFF	0xCA	65482	19212.96296	-0.067%
	38400	0xFF	0xE5	65509	38425.92593	-0.067%
	57600	0xFF	0xEE	65518	57638.88889	-0.067%
	115200	0xFF	0xF7	65527	115277.7778	-0.067%

NOTE: RHx and RLx setting value base on baud rate formula 4 (SMOD =1) or 5

N76E003 provide two bytes SFR to user trim HIRC value, default after reset the value is trim to 16MHz, once modify this SFR, the HIRC value will change. Suggest decrease reset value 15(dec.) will trim HIRC to 16.6MHz.

Following two Byte combine the 9 bit internal RC trim value. Each bit deviation is 0.25% of 16MHz that means about 40KHz / bit.

RCTRIM0 –High Speed Internal Oscillator 16 MHz Trim 0

7	6	5	4	3	2	1	0
HIRCTRIM[8:1]							
R/W							

Address: 84H Reset value: 16MHz HIRC value

RCTRIM1 –High Speed Internal Oscillator 16 MHz Trim 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	HIRCTRIM.0
-	-	-	-	-	-	-	R/W

Address: 85H Reset value: 16MHz HIRC value

Following is the demo code to modify HIRC to 16.6MHz,

```
sfr RCTRIM0         = 0x84;
sfr RCTRIM1         = 0x85;
bit BIT_TMP;

#define set_IAPEN   BIT_TMP=EA;EA=0;TA=0xAA;TA=0x55;CHPCON|=SET_BIT0 ;EA=BIT_TMP
#define set_IAPGO   BIT_TMP=EA;EA=0;TA=0xAA;TA=0x55;IAPTRG|=SET_BIT0 ;EA=BIT_TMP
#define clr_IAPEN   BIT_TMP=EA;EA=0;TA=0xAA;TA=0x55;CHPCON&=~SET_BIT0;EA=BIT_TMP

unsigned char hircmap0,hircmap1;
unsigned int trimvalue16bit;

void MODIFY_HIRC_VLAUE(void)
{
       set_IAPEN;
       IAPAL = 0x30;
       IAPAH = 0x00;
       IAPCN = READ_UID;
       set_IAPGO;
```